A New Small-Signal Model for Current-Mode Control

Raymond B. Ridley

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Before this book was written in 1990, there was a great deal of confusion about how to analyze power supplies which used the peak value of the switch current to regulate the output. Existing average models could not explain the high-frequency subharmonic oscillations that were observed. Attempts at modeling in the discrete-time domain yielded results too cumbersome for everyday design. And prominent researchers of the time disagreed on how the system should even be measured.

Two important pieces of work were combined to arrive at the conclusions in this book - the PWM switch model which very elegantly unifies all the PWM power stages into a single representation, and sampled-data modeling. The results are then simplified into an easily used form for design purposes.

In the years since this work has been published, other researchers have used alternate analytical approaches to verify the results. None of these other models have improved on the accuracy or simplicity of the results. Use of the analytical results in this book still provides the most accurate modeling available for peak current-mode control.

A recently added paper at the end of this book distills the crucial results into a concise and easy-to-read form. For the practicing engineer, this appendix is all you really need to know. For those interested in the details, history, and derivations, you are encouraged to read the whole book.

Ray Ridley, July 1999. Updated July 2018
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A NEW SMALL-SIGNAL MODEL FOR CURRENT-MODE CONTROL

by

Raymond B. Ridley

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in

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APPROVED:

Fred C. Lee

Fred. C. Lee, Chairman

Vatché Vorpérian

Bo H. Cho

Dan Y. Chen

Douglas J. Nelson

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1. Introduction

Current-mode control has been used for PWM converters for over twenty years. Despite this, there has yet to be a simple, accurate model that can predict all of the phenomena of current-mode control, and still be useful for design insight. Many variations of average analysis techniques have been presented which predict some of the observed low-frequency effects, but the models fail to provide accurate analysis at high frequencies. Accurate high-frequency modeling is es-pecially important for current-mode control since the most popular implementa-tion used today has an inherent instability at exactly half the switching frequency. This is easy to explain with pictures of circuit waveforms, or simplified discrete-time analysis, but the effect has not been incorporated into the average small-signal models.

More complex analysis techniques have been applied in the past, but although they could provide accurate modeling, their complexity prevented their wide-spread use by the engineering community.

This dissertation is an effort to provide a new small-signal model for current-mode control which is as easy to use as simple average models, but which pro-vides the accuracy required from sampled-data analysis. Approximations are applied to provide reduced-order models for the high-frequency analysis, and this results in very simple expressions which can be used for analysis and design.

1.1 Dissertation Outline

Chapter 2 of this dissertation reviews some of the many possible implementations of control schemes where the inductor current is part of the feedback process. The type of control analyzed here uses the *instantaneous* value *of* the inductor current once in every switching cycle to control either the turn-on or the turn-off of the power switch. Four modulation schemes are addressed, including the most commonly-implemented control where a clock is used to turn on the power switch, and the modulator compares the current signal to a control signal to turn off the switch.

The PWM switch model is an integral part of the new current-mode control model. In this work, a philosophy is taken that the power stage itself is not changed by the presence of a feedback circuit. The small-signal model for the power circuit does not change with current-mode control, and all of the open-loop power stage transfer functions can be extracted from the model. The duty cycle

remains as a variable which can be observed. All of the effects caused by current-mode control are accounted for by a new *control-circuit* model which is then connected to the existing power stage.

The final section of Chapter 2 reviews some of the existing small-signal models for current-mode control. The essential differences in the approaches are pointed out, and transfer functions are presented to show where some of the average models break down. Early sampled-data modeling is referenced since this approach was started before but never completed due to its apparent complexity.

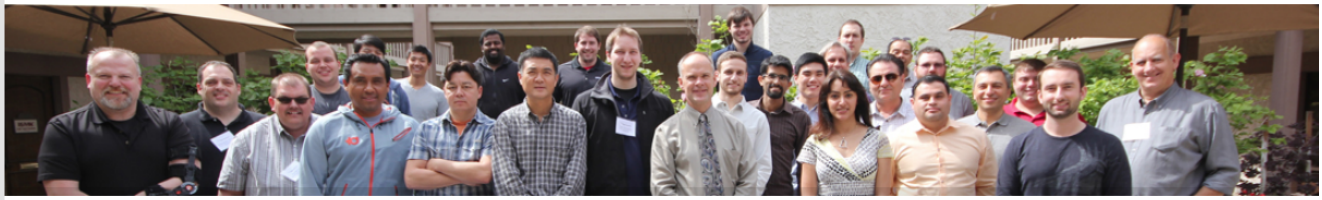
The high-frequency modeling techniques that are needed for the current-mode system do not need to be applied to the complete power stage. There is no benefit in involving slowly-varying states in the sampled-data modeling process at all, since analytical results cannot then be extracted. Chapter 3 identifies the current-mode cell of all PWM converters that use current-mode control. The slow filter states surrounding the controlled inductor current are fixed, and sampled-data analysis is performed on the resulting first-order system. This provides a compact expression for an equivalent sampling gain term which can be placed in the feedback model.

In Chapter 4, the sampling gain term is approximated by a simple second-order expression. The slowly-varying states surrounding the current-mode cell are then allowed to interact with the sampled-data model, and the derivation of two additional gains completes the new current-mode model. Converters which operate

in the discontinuous mode are also addressed in this chapter, and it is shown that no sampled-data modeling is needed. The model of the power stage is coupled with just one feedforward gain to provide the DCM model.

The results of the new current-mode model are applied to some examples in Chapter 5. A buck converter was selected since it has some of the most interesting characteristics with current-mode control. Approximate analytical transfer functions are derived for the converter and it is shown that the best model for the control-to-output-voltage transfer function is ***third-order***. This is a significant new result which explains why previous two-pole or single-pole average models could never give satisfactory results. Predictions of the new model are confirmed with experimental measurements for several different modes of operation. Simple equations are provided to help with the design of the feedback.

Conclusions are presented in Chapter 6. For those readers who wish to extract the fundamentals of this dissertation, and use the results without reading the whole work, a concise summary of the new current-mode model is provided in Appendix A. All of the parameters derived in the dissertation are provided to allow application of the model. Appendix B is provided to show how the new model can be easily implemented into PSpice, a circuit analysis program. A sim-ple invariant subcircuit is given which can be used for the simulation of the small-signal characteristics of PWM circuits using either voltage-mode or current-mode control. These two appendices, coupled with the design insights of Chapter 5, provide the reader with immediately useful design tools.



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- Learn how to measure control transfer functions and optimize loops for single and multi-loop converters at power levels to 10 kW.

2. Review of Existing Models

2.1 Introduction

There are many different control schemes which use the inductor current signal in one way or another to control the power converter, and all of these could be defined as current-mode control. Some of the different implementations which have been used in the past are described in this chapter. The specific control schemes which are the most widely used today, and which have eluded, accurate and simple modeling in the past, are addressed. The instability which can exist in the current feedback loop is presented.

A brief review of power stage modeling using the three-terminal PWM switch model is given. This provides a simple power stage model which allows compar-ison of existing analysis techniques and which is used as part of the new current-mode control model.

Finally, this chapter presents a brief summary of existing modeling techniques for current-mode control which have been used in .the past. The shortcomings of average models in the high-frequency domain are shown.

2.2 Implementations of Current-Mode Control

There are many different ways to use the inductor current of a converter as part of the feedback mechanism and control system. Different forms of current mode control can be found in references as early as 1967 [1]. This dissertation addresses the analysis of a subset of the many different implementations of current-mode control.

Prior to current-mode control, the most common control circuit for PWM converters used voltage-mode, or single-loop control. Fig. 2.1 show the most popular implementation of this control. A fixed-frequency clock is used to turn on the power switch of the PWM circuit. At the same time, a sawtooth ramp, with slope S_e, is initiated, and this ramp intersects a control voltage, v_c, to terminate the on-time of the power switch. The sawtooth ramp is reset to zero at the end of the switching cycle. Many different integrated circuits are available to provide this control function for PWM converters.

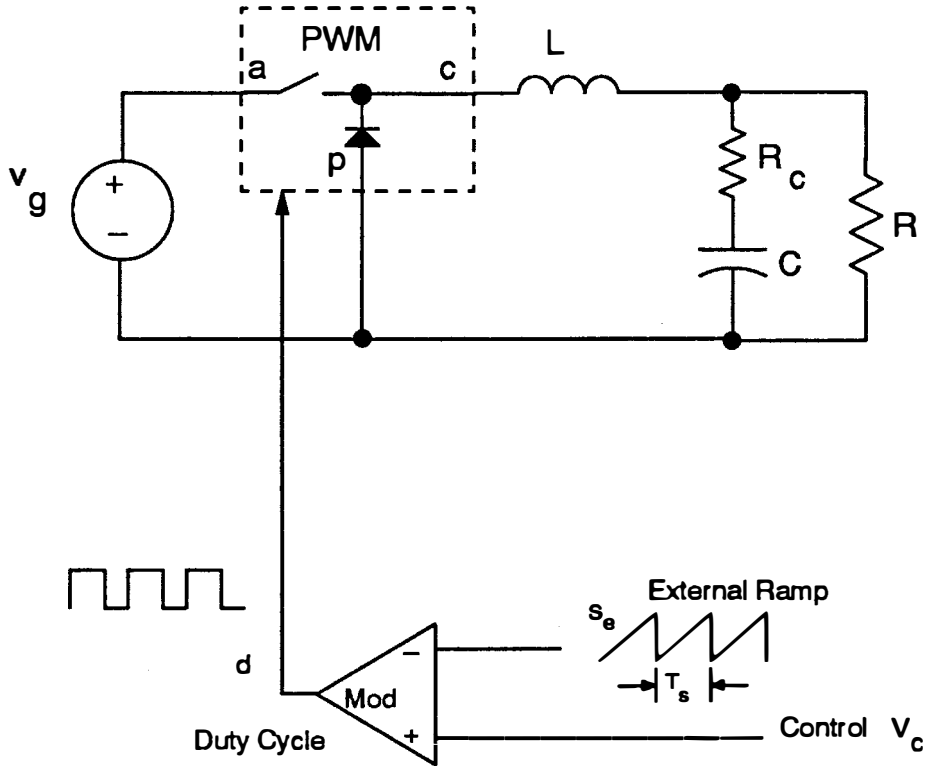


Figure 2.1. Buck Converter with Voltage-Mode Control: *The duty cycle control signal is provided by a sawtooth ramp intersecting a control voltage threshold. The model for this control system is well represented by existing average techniques, provided that the control signal is continuous.*

In the late sixties and early seventies, there was a strong motivation to use naturally-occurring waveforms in a power circuit to generate control functions. Integrated circuits for control were not available, and the use of discrete circuits and low-level integrated circuits became very complicated. A patent issued in 1967 to Gallaher [l] describes a circuit using only a comparator and a Schmitt trigger to control the switching of a buck converter. Ramp waveforms provided by the de and ac inductor current signals provided hysteretic control of the converter.

The general implementation of hysteretic current-mode control is shown in Fig. 2.2. The inductor current waveforms are used to control both the turn-on and the turn-off of the power switch of the PWM converter. The advantages of this kind of circuit are apparent: no clock or timing function is needed, and the current level is controlled between two limits. Although this implementation was popular before control circuits became available, its variable switching frequency, and the need to sense the inductor current during both the on- and off-times of the power switch have restricted its use today. This circuit does not have any problems with instability of the current-feedback loop, and it is not analyzed in this dissertation. A small-signal model was presented in [2] which predicts the essential dynamics of the system.

A patent issued in 1972 to Schwarz [3] describes a technique for generating digital control waveforms, such as those needed for a switching converter, by integrating naturally occurring analog waveforms in a power circuit. The original implemen-

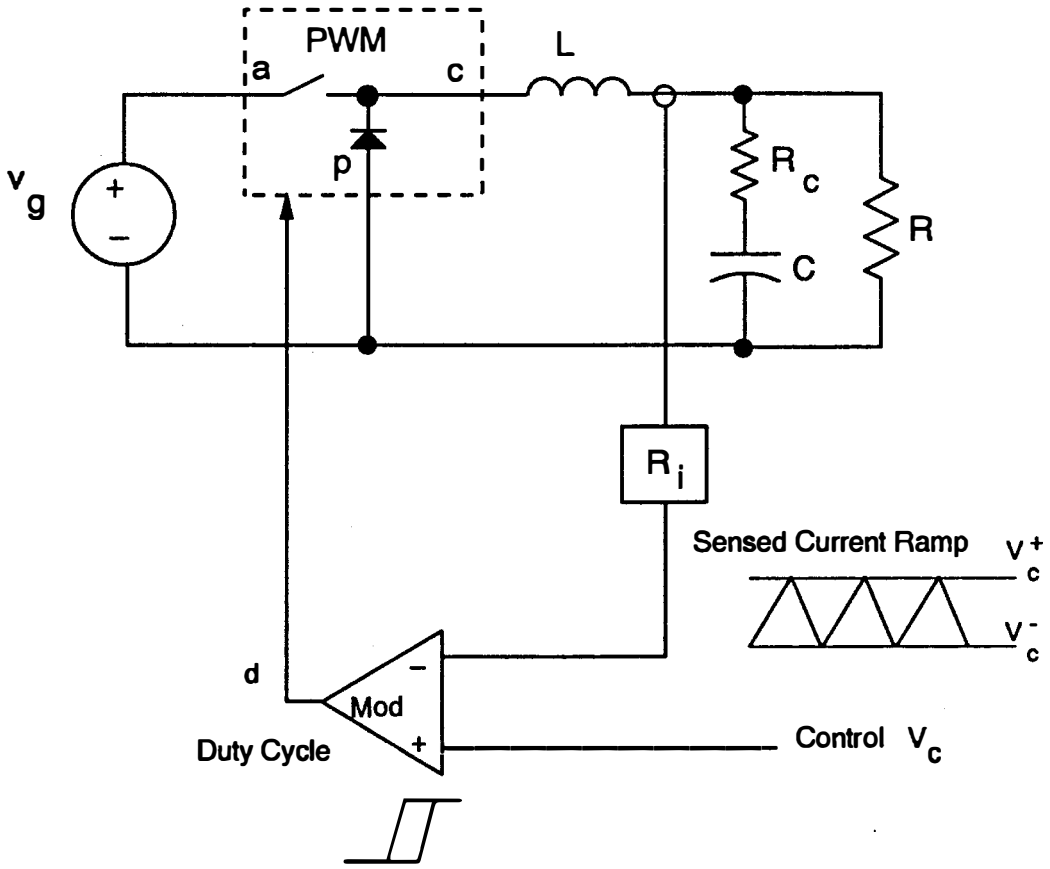


Figure 2.2. Buck Converter with Hysteretic Current-Mode Control: *A control signal is used with a hysteresis band to determine the turn-on and turn-off times of the switch. No external clock or ramp is needed. This approach is not analyzed in this dissertation.*

tation of this was for resonant converters. This technique was applied to PWM converters in [4], where the voltage across the inductor is integrated to provide a control waveform. Fig. 2.3 shows the implementation of this control scheme for an example buck converter.

The modulator for this circuit is very similar to that for voltage-mode control. The modulator ramp is implemented with the current signal obtained by itite-grating the inductor voltage. For constant-frequency modulation, an external ramp is still used in the modulator to prevent instabilities inherent in this system. This is discussed later in this chapter. The circuit implementation used in this figure later became known as the "standardized control module" (SCM) imple-mentation since its form is the same for any topology PWM converter. The con-trol scheme provides all of the benefits of current-mode control except for current limiting and current sharing between parallel modules. The de information about inductor and switch current is lost in the control scheme. However, it does pro-vide some advantages in terms of signal-to-noise performance, and this is dis-cussed in [5-6]. The control scheme is still used by many people.

The most common form of current-mode control was published in a paper by Deisch in 1978 [7]. The basic elements of this control scheme, commonly called "current-injection control" (CIC), are shown in Fig. 2.4. The active switch cur-rent is sensed instead of the inductor current. The switch current is equal to the inductor current during the on-time, and the effect is the same as if the inductor current were sensed directly. The advantage of sensing the switch current is that

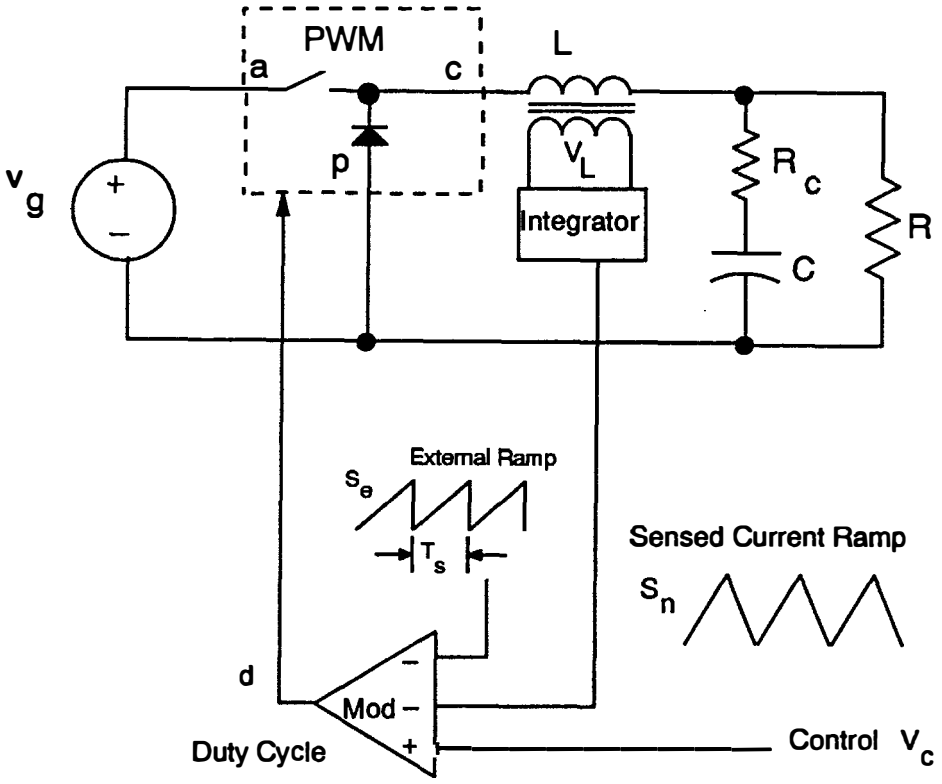


Figure 2.3. ***Buck Converter with "SCM" form of Current-Mode Control:*** *A signal proportional to the inductor current is derived by integrating the voltage across the filter inductor. This approach provides a continuous current signal during on- and off-times of the switch, but dc information is lost.*

a current transformer can be used, providing a large signal without the significant power dissipation that would be encountered with a current-sense resistor.

Both the SCM and CIC implementations of current-mode control are identical in terms of their small-signal performance. The fact that the SCM control does not carry de information is due to integrator offsets and nonlinear limits on the inductor-voltage integration process. Both of the control schemes sense the inductor current, scale it with some arbitrary gain, referred to in this dissertation as R_i, and use the signal as part of the modulator. Fig. 2.5 shows the current-mode modulator removed from the specific converter. With SCM control, the current-sense waveform is continuous. With CIC control, the current during the off-time of the power switch can be reconstructed, if necessary, by sensing the current through the passive switch of the circuit.

Many different modulation strategies can be implemented where the inductor current is used. The most commonly-used approach is to use a constant-frequency clock to turn on the power switch, and use the intersection of the current signal plus the external ramp with the control voltage signal to turn off the power switch. This modulation strategy is shown in Fig. 2.6a. It is sometimes referred to as constant-frequency, trailing-edge modulation.

Another constant-frequency modulation scheme uses a clock signal to turn *off* the power switch, and the inductor current to provide the turn-on signal. The

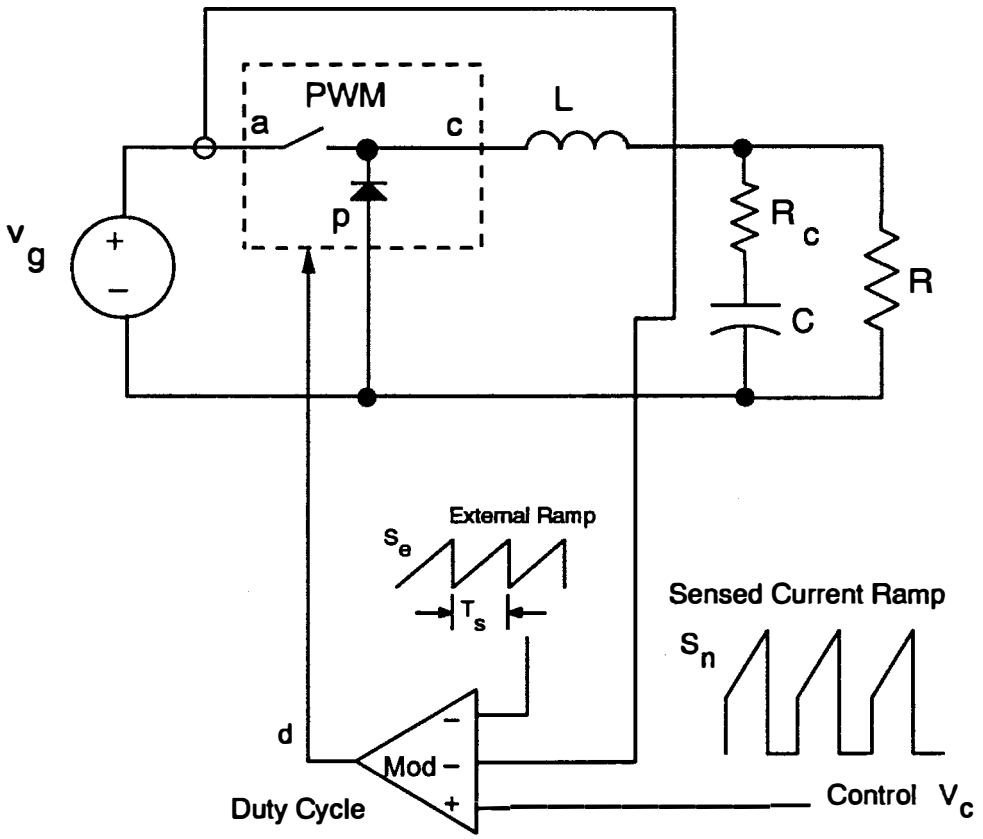


Figure 2.4. Buck Converter with "CIC" form of Current-Mode Control: *In this scheme, the inductor current is sensed by a current transformer in series with the power switch. The current information is only available during the on-time of the switch. The de information of the current is preserved in this approach, providing inherent current limiting and current sharing of multiple modules.*

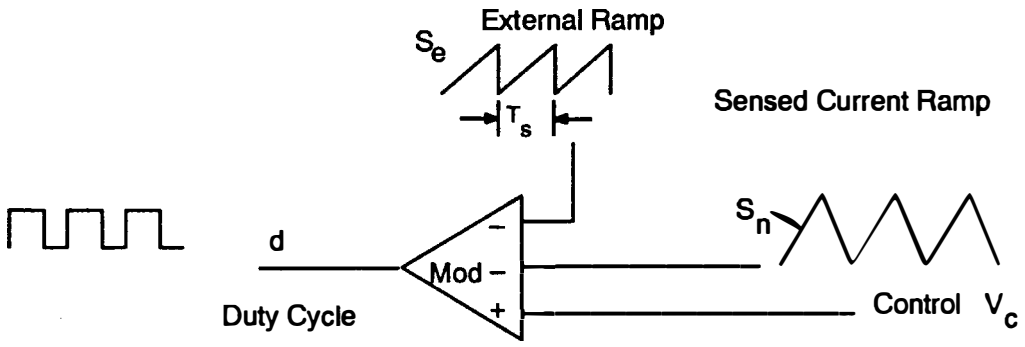
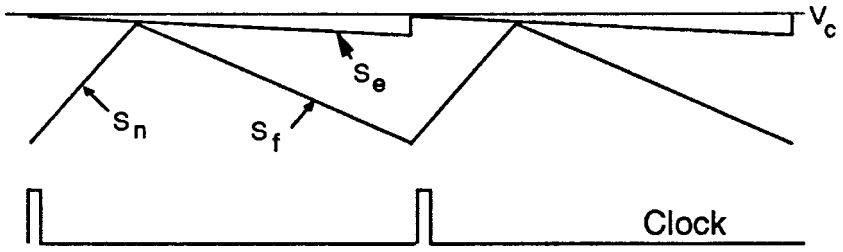
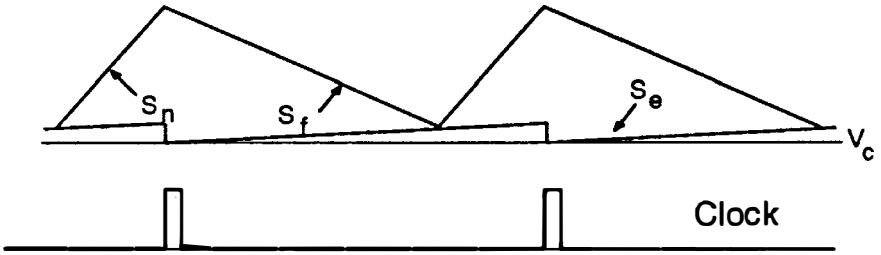


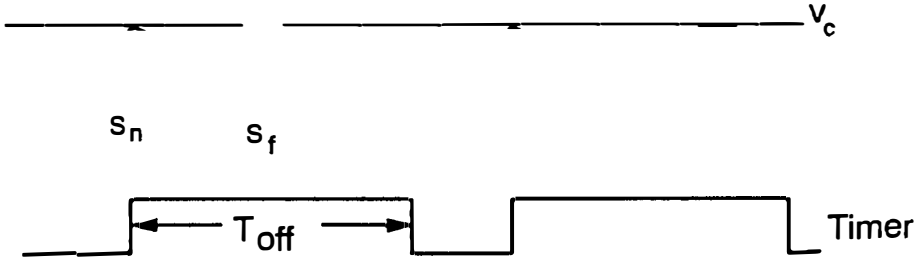
Figure 2.5. Basic Structure of Current-Mode Controller: *Regardless of the current-sensing technique, both the CIC and SCM control achieve the same effect. The current signal is summed with an external ramp and compared with a control signal to provide the duty cycle to the power stage.*



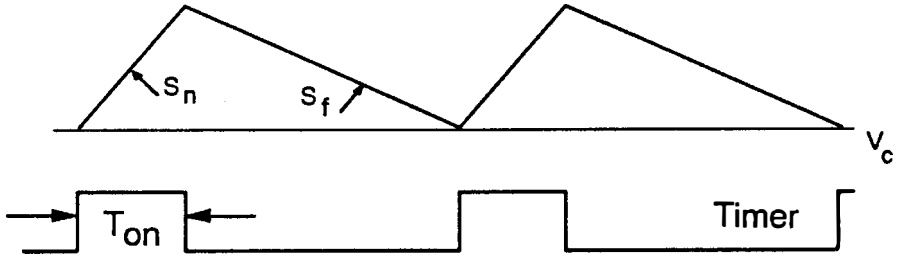
(a) Constant-frequency control, clock initiates on-time



(b) Constant-frequency control, clock initiates off-time



(c) Variable-frequency control with constant off time



(d) Variable-frequency control with constant on time

Figure 2.6. Different Modulation Schemes for Current-Mode Control: *Four of the many possible modulation schemes are shown in this figure. Constant-frequency control with a clock initiating the on-time of the power switch is the most commonly-used approach.*

waveforms for this scheme are shown in Fig. 2.6b. This modulation scheme requires inductor current information during the off-time of the power switch, and can only be implemented with SCM control, or with CIC control if the diode current is sensed. The modulation strategy is the dual of the other constant-frequency scheme, and is analyzed in this dissertation by default. The control scheme is sometimes referred to as constant-frequency, ***leading-edge*** modulation.

The controller does not need to be run at constant frequency. A modulation scheme can be used where the off-time of the switch is fixed with a timer, and the switch is turned off with the modulator current signal. This is referred to a constant off-time control, and the waveforms for the specific implementation analyzed in this dissertation are given in Fig. 2.6c. There are many different ways to implement variable-frequency modulation schemes, and many of these are commonly used in communication theory [8,9].

The final form of current-mode control analyzed is the dual of constant off-time control, and shown in Fig. 2.6d. The power switch is turned ***on*** for a constant period, and the turn-on instant is governed by the modulator, using the current ramp. Like the constant-frequency, leading-edge modulation scheme, this control is more difficult to implement and not commonly used, but it is analyzed for completeness.

In 1977, a patent was issued to Hunter [10] for a control scheme where the switch current waveform was integrated. Such low-pass filtering was recently discussed

in [11] in light of power-factor correction circuits, and some of the advantages of the scheme were presented. This type of control falls into a class referred to here as "average" current-mode control, where the controlled current is processed by a low-pass filter. The scheme is conceptualized in Fig. 2.7. If sufficient filtering is used, so that the filtered current waveform does not have any significant ripple, average current-mode models can be used for analysis. The class of control becomes interesting when the filtering is less, and the switching ripple is still comparable to the external ramp size, but the analysis of this is beyond the scope of this dissertation.

2.3 Power Stage Modeling with the PWM Switch

Before reviewing existing current-mode models, it is important to review the modeling of the power stage of PWM converters. Traditionally, this analysis has been done through the technique of state-space averaging [12-14]. However, a recent advance in converter modeling was presented in [15] to greatly simplify the analysis procedure. An accurate and elegant circuit model results which is in-variant for all PWM converters where a common nonlinear switching function can be defined.

Fig. 2.8 shows the commonality of the three basic PWM converters. In each of these converters, the nonlinear switching action can be confined to a three-

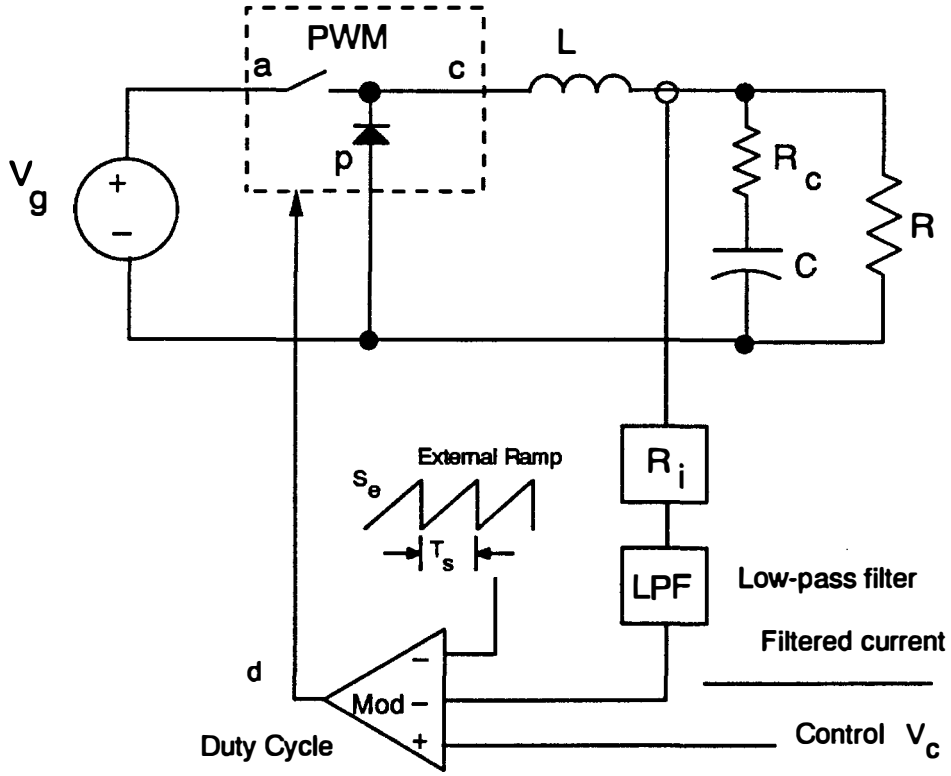


Figure 2.7 "Average" Current-Mode Control: *The sensed inductor current, or switch current, is processed by a low-pass filter. If the filtering is sufficient, average models work well for this scheme. This is not analyzed in this dissertation.*

terminal circuit element containing the power switch and diode. The connection of the element at the power switch is referred to as the active terminal, and the connection at the diode is referred to as the passive terminal. The third terminal, which is connected to both switches, is referred to as the common terminal. The orientation of the diode will depend upon the de conditions of the external circuit, but this does not affect the modeling. The definition of the polarities of the com-mon current and terminal voltages will account for the orientation. The identifi-cation of this invariant structure greatly simplifies the small-signal analysis of the power stage, and Vorperian showed in [15] that it is unnecessary to carry the ex-ternal states of the converter into the analysis.

The result of the PWM switch analysis is a simple equivalent small-signal model which replaces just the nonlinear switching elements of the PWM converter. The simple form of the PWM switch model is shown in Fig. 2.9. The sources of the switch model determined by the steady-state inductor current, I_c, out of the common terminal, the steady-state duty cycle, D, and the steady-state voltage across the active-to-passive terminals, V_{ap}. These quantities are easily determined by the de conditions of the power stage. More elaborate versions of the switch model were presented in [15] to include discontinuous waveform effects, and storage-time modulation. The differences in the model are not significant for the purposes of this dissertation, but readers wanting to use these models can incorporate these enhancements into the new current-mode model with good results.

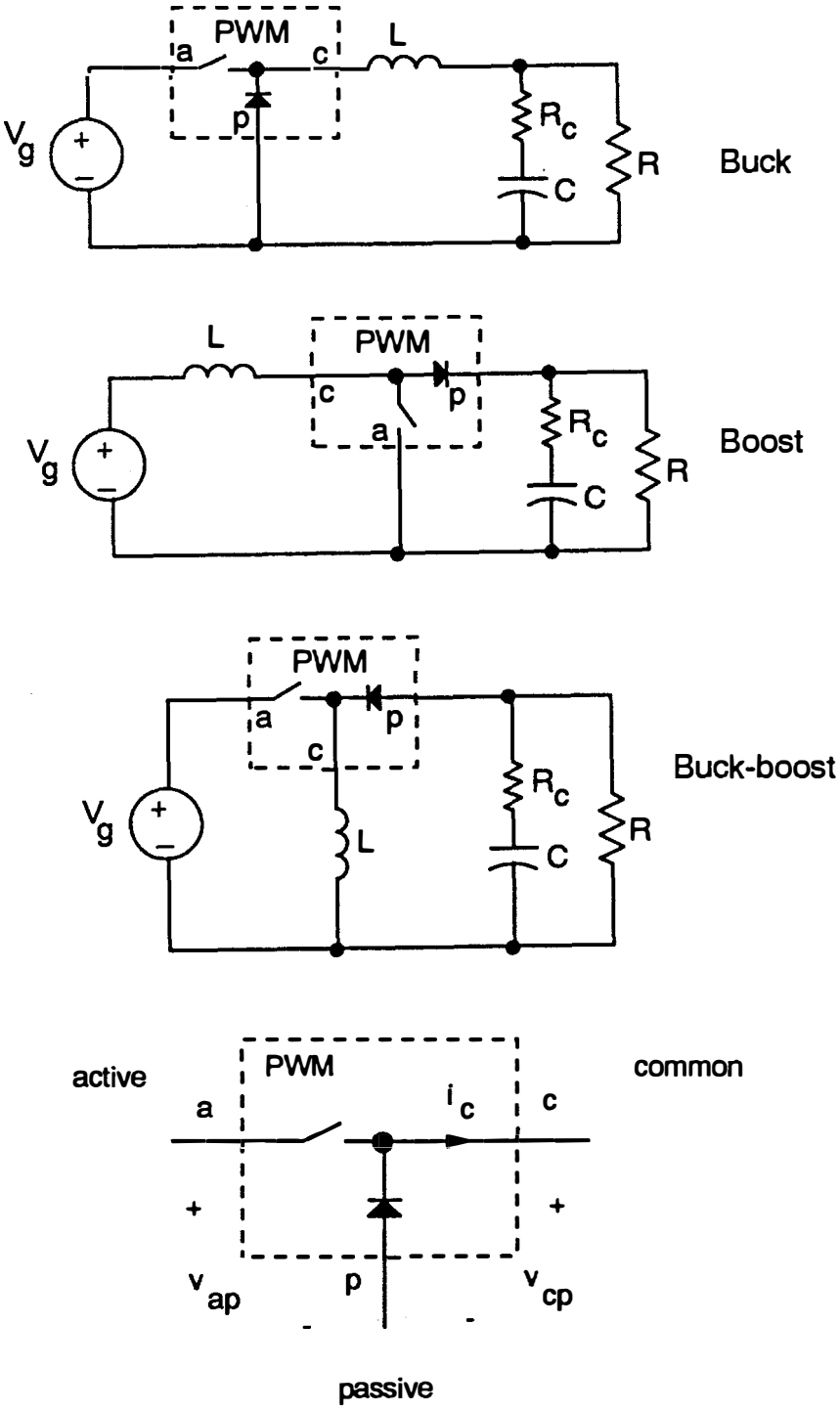


Figure 2.8. Basic Converters with Switch Definitions: *An invariant nonlinear block can be identified for most PWM converters. The terminal with the controlled switch is called the active terminal, the diode is connected to the passive terminal, and the inductor is connected to the common terminal. The diode orientation will change according to the polarity of the common terminal current.*

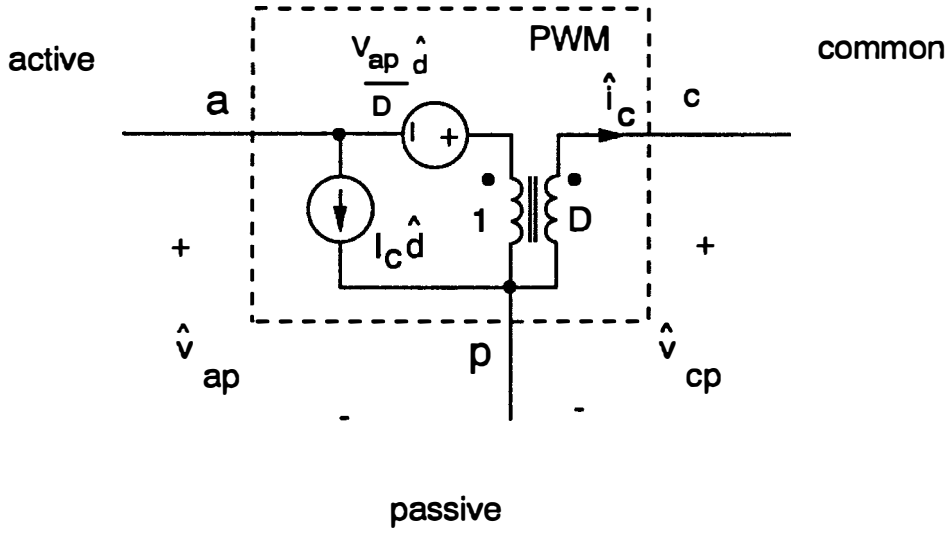


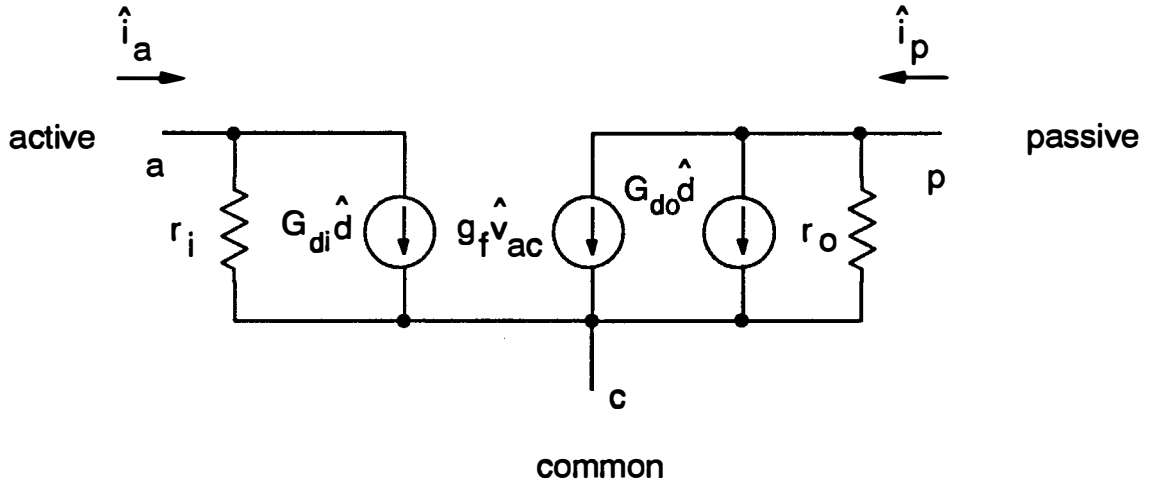
Figure 2.9. PWM Switch Model for Continuous-Conduction Mode: *This invariant model replaces the nonlinear switching block in the PWM converters to provide a simple, convenient small-signal model.*

The small-signal switch model is simply substituted into the PWM converter with its terminals appropriately oriented. A most attractive feature of the PWM switch model, compared to previous circuit models, is that it preserves the original circuit structure and component values. Only the switching elements are replaced.

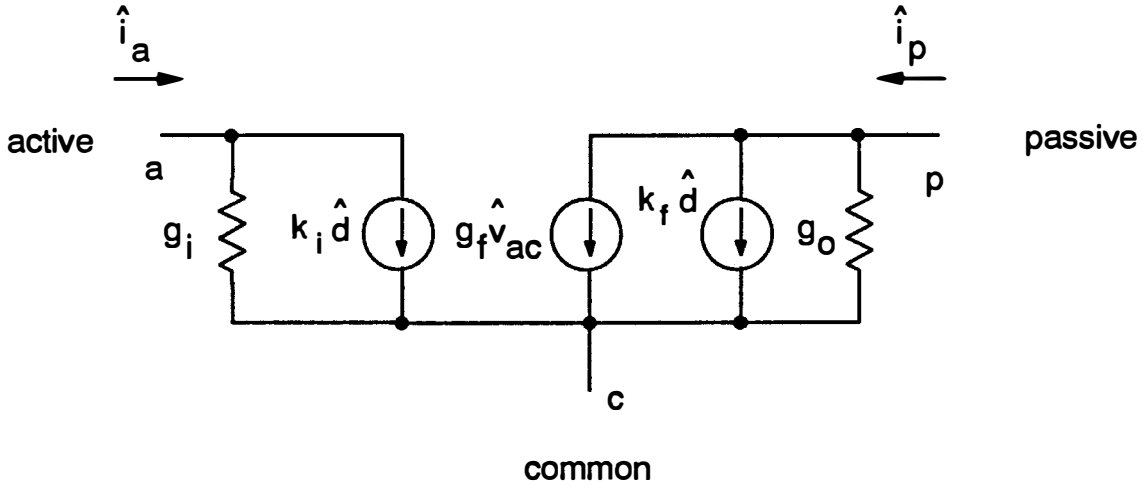
When the circuit operates in discontinuous-conduction mode, a different small-signal results for the three-terminal PWM switch. The form of this model is shown in Fig. 2.10. As with the continuous-conduction model, the sources and components of the small-signal equivalent circuit are determined from the steady-state circuit values. It is important to point out that the notation of the DCM model has been changed from the original *g*-parameter model presented in [15]. Changes have been made to provide a model with consistent units and component names which can be used directly in circuit modeling tools.

2.4 Existing Models for Current-Mode Control

The control schemes analyzed in this thesis have a specific problem that has caused great difficulty in the past in small-signal modeling for constant-frequency control. With no external ramp added to the control, the current in the circuit can oscillate at half the switching frequency. This problem is illustrated in Fig. 2.11. With trailing-edge modulation, and duty cycles less than 0.5, the oscillations decay. At duty cycles greater than 0.5, the oscillations grow larger until a limit-



(a) DCM model with notation used in this dissertation



(b) Original g-parameter model notations

Figure 2.10. PWM Switch Model for Discontinuous-Conduction Mode: *This invariant model replaces the nonlinear switching block in the PWM converters which operate in the discontinuous conduction mode. The notation used in this dissertation is consistent with units and PSpice circuit modeling, described later. The notation is different from the original g-parameter model presented in [15], and shown in the lower circuit.*

cycle mode is reached. Such a mode of operation is undesirable in a power converter.

Average models are usually used for the analysis of current-mode systems. The structure of these models is shown in Fig. 2.12. The power stage can be modeled by state-space averaging, or with the PWM switch model. The inductor current feedback is modeled with a simple gain term, R_i, which is simply the current-sensing gain of the circuit. *Differences in particular models arise in the derivation of the gain of the modulator,* F_m, and in the presence of feedforward gains from the input and output voltages to the duty cycle.

One of the earliest models was developed by Lee in [16] to provide a model for SCM control. This particular model had no feedforward terms, and an interesting form of the modulator gain:

$$F_m = \frac{2}{\left(S_n - S_f + 2S_e\right)T_s} \tag{2.1}$$

where S_n is the magnitude of the slope of the sensed current ramp used by the modulator during the on-time of the switch, S_f is the magnitude of the slope of the sensed current ramp during the off-time of the switch, and S_e is the slope of the external ramp added to the modulator. This modulator gain has the characteristic of becoming very large as a duty cycle of 0.5 is approached when no external ramp is added to the system. This modulator model was also used in [5,6], resulting in some incorrect design observations in regard to external ramp effects

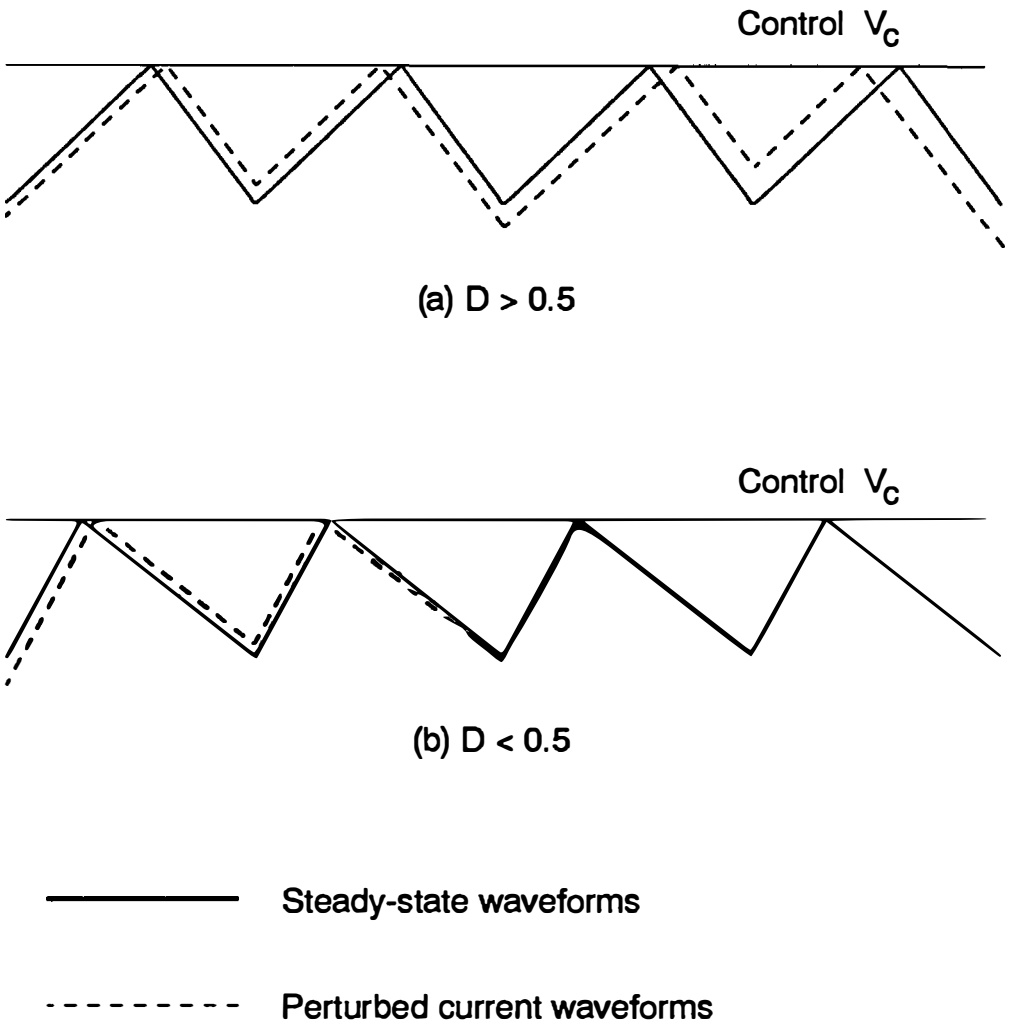


Figure 2.11. Instability Observed with Constant-Frequency Controller: *With fixed-frequency control, and the clock initiating the on-time of the active switch, the closed current loop exhibits oscillatory behavior at half the switching frequency. This oscillation is damped at duty cycles below 0.5, and grows with larger duty cycles.*

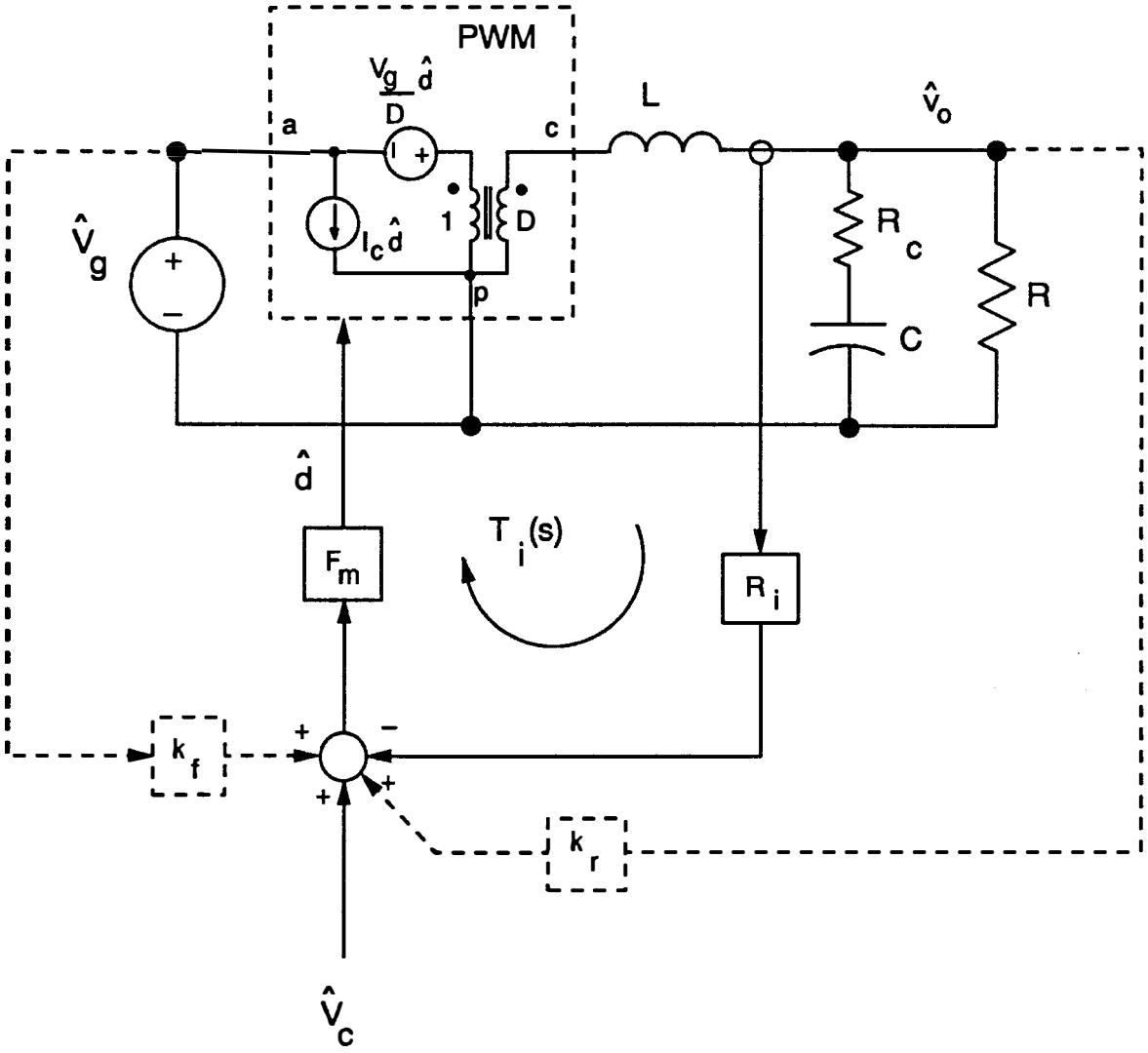


Figure 2.12. Average Current-Mode Control Models: *The PWM switch is used to generate the power stage model. There are no frequency-dependent terms in the feedback of the inductor current. Some average models incorporate feedforward terms from input and output voltages.*

in [5]. It was suggested in [5] that the addition of a small external ramp to a system would change the crossover frequency of the current loop by an order of magnitude, eliminating many of the benefits of current-mode control. It will be shown in this dissertation that the current-mode system is not this sensitive to external ramp addition, and the benefits of current-mode control can be significant even with a large external ramp.

A second popular approach to analyzing the current-mode system was presented in [18] by Middlebrook. In this model, the presence of feedforward terms was shown. The importance of these terms will be shown in Chapter 5 where the new current-mode model, which also has feedforward terms, is applied to some specific converters. The modulator gain for the models in [18] was found to be:

$$F_m = \frac{2}{(S_n + 2S_e)T_s} \tag{2.2}$$

This gain is significantly different to that of Eq. (2.1), especially when no external ramp is used. With a large external ramp added to the modulator, both of the gains of Eqs. (2.1-2.2) become the same. A third model, given in [20] finds the modulator gain to be:

$$F_m = \frac{1}{(S_n + S_e)T_s} \tag{2.3}$$

The importance of these different modulator gains, and the explanation for the apparent success of these diverse models will be presented later.

All of the models have a common feature. With a reasonably-sized external ramp, the inductor current feedback loop has a high crossover frequency. At frequencies well below the crossover frequency, the inductor current of the models can then be assumed to behave like a current source, and the inductor current is eliminated as a state in some models. With this assumption, a simple circuit model can be derived which predicts the dominant-pole behavior of the current-mode system. This circuit model is shown in Fig. 2.13.

Most other popular modeling approaches [21-26] follow the average model derivations with minor deviations, and arrive at models which have both power stage states with feedback of the inductor current, or a reduced power stage with the inductor current eliminated. A recent paper [27] reexamined work done in [18] to again derive a single-pole model after modifying some of the analysis.

The lack of a single current-mode model which is used universally is due to the simple fact that *none* of the average modeling techniques described here can adequately explain the phenomena observed with current-mode control. Of course, it is unreasonable to expect that a model which averages circuit waveforms could accurately predict all of the phenomena which occur in a current mode system where the instantaneous value of a state is used for control. In particular, the oscillation which can occur at half the switching frequency could not possibly be accurately accounted for with an average model. Average models are usually supplemented with an explanation of circuit waveforms to show how an external ramp could be added to avoid the instability, but the effect is not incorporated

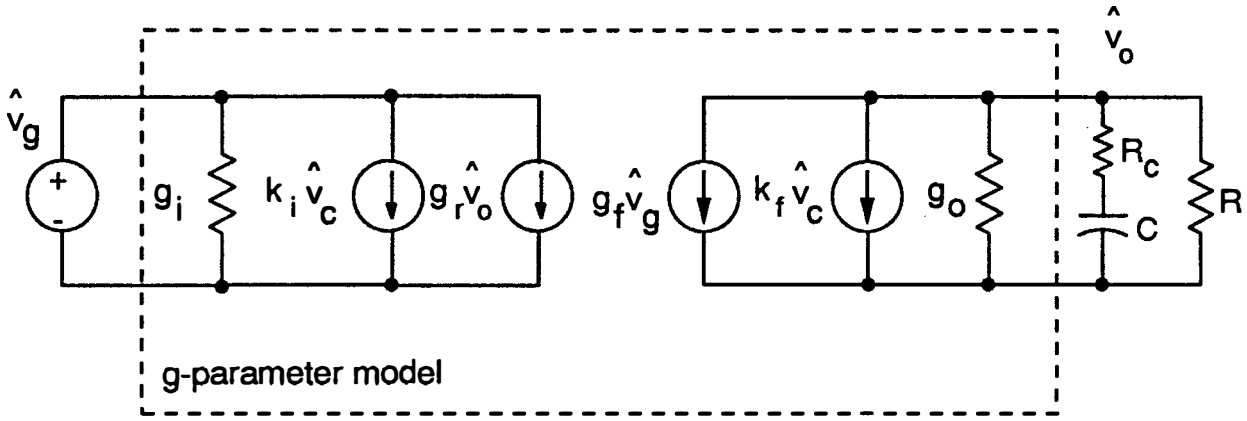


Figure 2.13. Simplified Average Current-Mode Control Model: *Many previous modeling approaches assume that the current loop has sufficient gain and high enough crossover frequency to allow the low frequency model to be reduced to a single-pole model, without the inductor current.*

into the small-signal model. An observation made in [24] touched on the nature of the problem: the instability observed is characteristic of a system with high-Q second-order poles. The accuracy of this observation will be seen later in this dissertation.

Recognizing the shortcomings of average models to predict the instability of current-mode control, Brown [28,29] applied sampled-data techniques to analyze the problem more rigorously. Continuous-time expressions were found for a buck converter, with the output capacitor replaced with a voltage source, as shown in Fig. 2.14, and the instability in the current loop was demonstrated. (The analysis was actually done for the buck converter with the output capacitor state included, but analytical results were found for the high-frequency region only, where the capacitor can be considered to be a short circuit.) However, even this reduced-order model was thought to be too complex for analytical insight, and the technique was abandoned in favor of discrete-time analysis.

Other researchers have also applied discrete-time analysis to the problem [30-32], using numerical techniques to produce transfer function bode plots. Fourier analysis techniques were applied in [33-34] to allow computers to plot transfer functions beyond half the switching frequency, but none of these techniques provide the analytical design insight required for good design.

Averaged models described above have been used with some degree of success in the past, which may seem surprising considering the differences in some of the

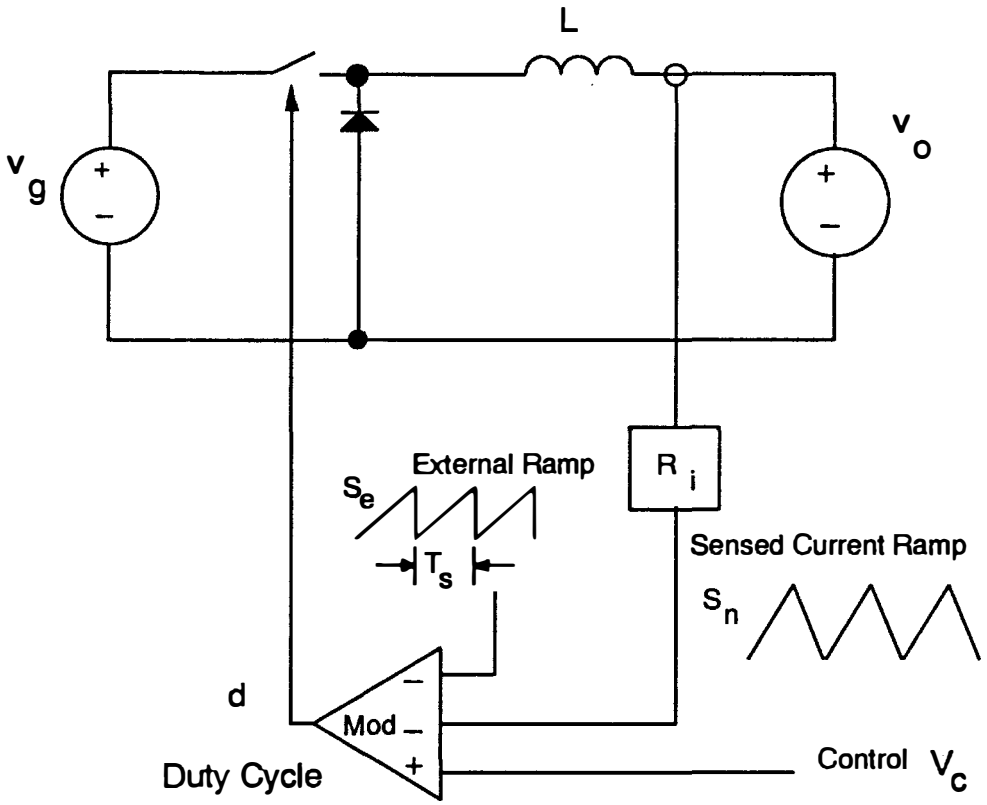


Figure 2.14. Sampled-Data Modeling Approach: *A simple buck converter was modeled at high frequencies using sampled-data techniques. This was able to explain some of the phenomena of current-mode control, but the complexity of the modeling led researchers to abandon this technique.*

models. Fig. 2.15 shows an example transfer function of two of the average models, [16] and [18], compared with the sampled-data model of [29], and measured data. At low frequencies, all of the models agree well with measurements. However, approaching half the switching frequency, the average model predictions differ significantly from the measured results. The measurements shown are for a constant-frequency converter operating with a duty cycle of 0.45.

Fig. 2.16 shows the measurement of the current feedback loop, T_i, as defined in Fig. 2.12. This transfer function clearly shows the differences in the models due to the different modulator gains given in Eqs. (2.1-2.2). Both the average models show a gain which is higher than the measured gain, and both models predict that the current loop can have a crossover frequency in excess of half the switching frequency. This is in conflict with Nyquist criteria for sampled-data systems. The model of [18] shows a 6 dB discrepancy from measurements when no external ramp is used. The discrepancy of the model of [16] can be much larger without an external ramp at duty cycles close to 0.5.

The apparently severe mismatch of the measurements and predictions of the current loop gains, however, have not prevented use of these models. This can be explained by the fact that the control-to-inductor current transfer functions, and the control-to-output-voltage transfer functions, contain the modulator gain of the model in both forward gain, and feedback gain paths. These transfer functions are of the form:

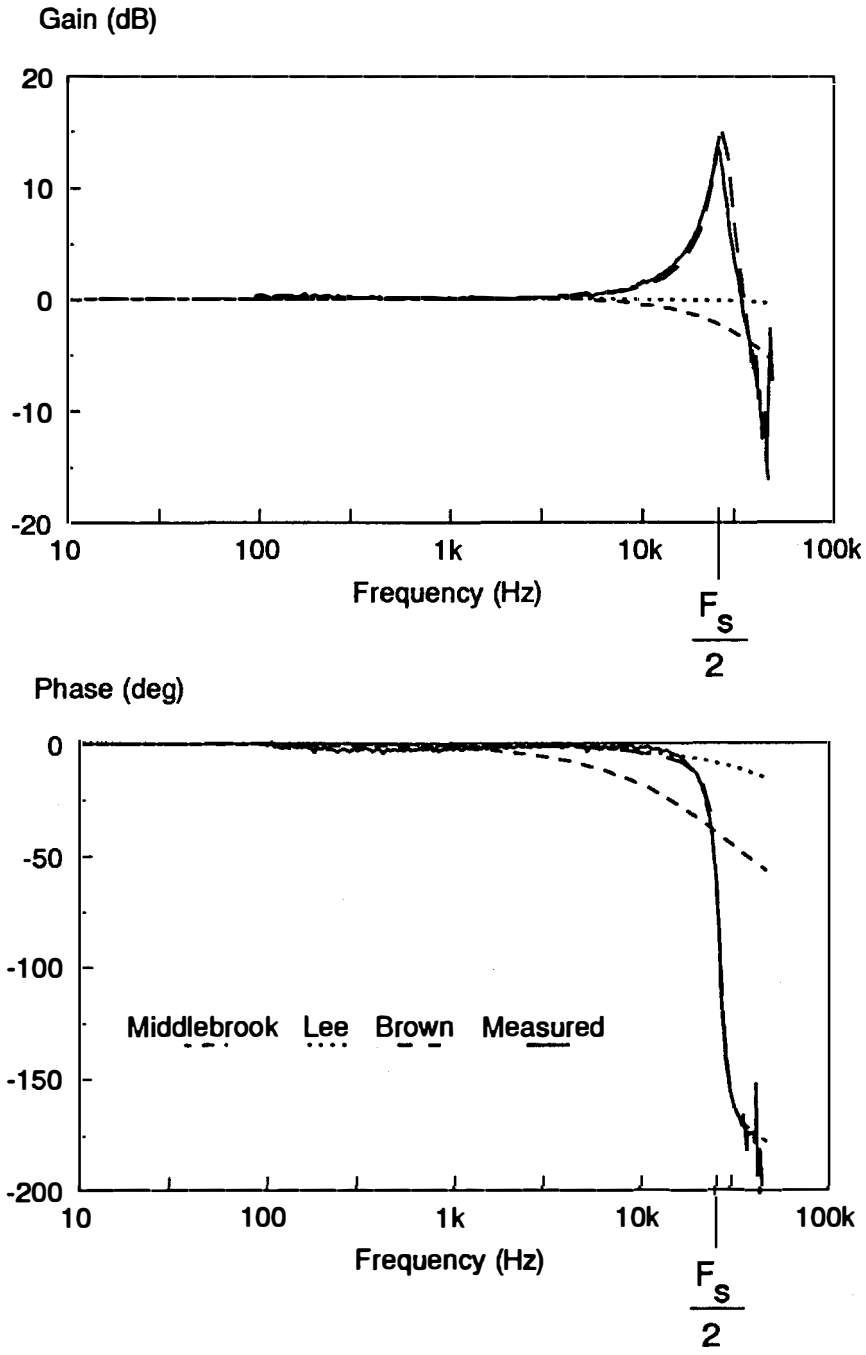


Figure 2.15. Predictions of Control-to-Inductor Current Transfer Function: *The control-to-inductor-current transfer function is plotted here for two of the average models, [16] and [18], and the sampled-data model of [29]. The significant deviations of the average models and the observed results at half the switching frequency are apparent.*

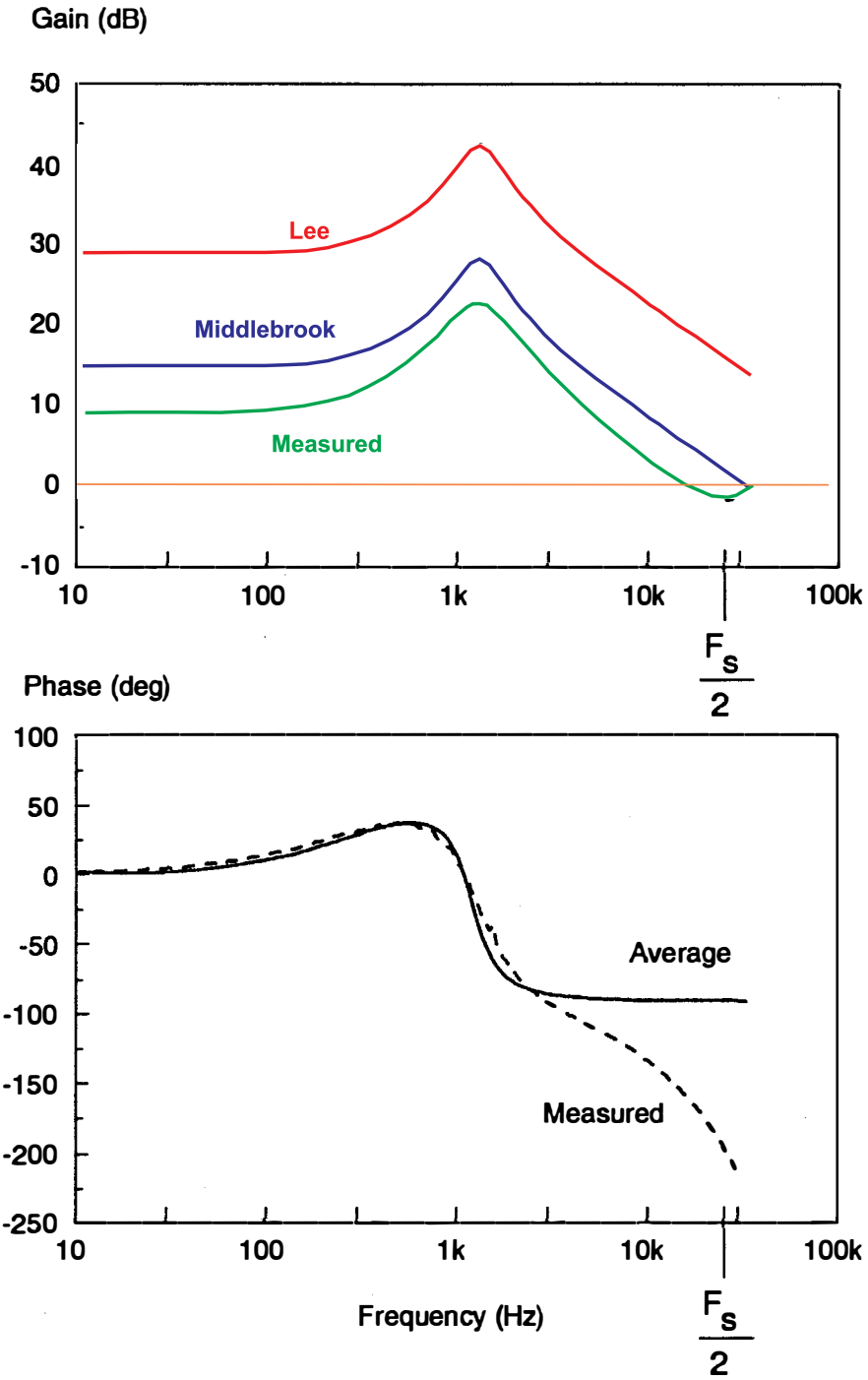


Figure 2.16. Predictions of Current-Loop Gain Transfer Function: *Significant differences in measured results and predictions of two averaged models are shown here. Notice that both of the average models would indicate that the current-loop crossover frequency can exceed the Nyquist frequency of the system, yet still remain stable, a violation of basic Nyquist principles.*

$$F(s) = \frac{F_m F_{ps}}{1 + F_i F_m R_i} \tag{2.4}$$

where F_{ps} is any power stage transfer function of interest and F_i, is the duty-cycle-to-inductor-current transfer function. At frequencies where the gain of the current loop is higher than unity, any errors in the predictions of the modulator gain are cancelled. This explains why the current loop gains Fig. 2.16 have significant errors, but the closed-loop gains of Fig. 2.15 are in good agreement at low frequencies.

2.5 Conclusions

There are many different ways to implement current-mode control, and some of these have been described in this chapter. This dissertation provides a new small-signal model for the common implementations of current-mode control where the instantaneous inductor current is used as part of the modulator. Four common modulation schemes will be analyzed, two with constant-frequency control, and two with variable-frequency control. Two of the schemes, constant-frequency with trailing-edge modulation and constant off-time control, will be analyzed in both continuous-conduction mode and discontinuous-conduction mode. The other two, constant-frequency with leading-edge modulation and

constant on-time control, are analyzed for continuous-conduction mode only, since these control schemes cannot operate in discontinuous mode.

Converters with constant-frequency control can be unstable when the current-loop is closed. This is easy to explain qualitatively from circuit waveforms, but the effect has not been incorporated into a simple small-signal model. When the model of this dissertation is developed and applied, it will become apparent why the average techniques failed to accurately model the system, and why this effect needs to be modeled properly. The instability that is observed is not an effect that suddenly appears for certain circuit conditions. The oscillations gradually become less damped approaching the instability point, and it is important to have an accurate model for all conditions. The underlying cause of the instability affects the system performance well before the system becomes unstable.

The three-terminal PWM switch model was reviewed briefly for continuous-conduction mode and discontinuous-conduction mode. This simple circuit model is used as a central part of the new current-mode model.

Finally, it was pointed out that widely-used models from Middlebrook and Lee have significant variation from each other, and there are large discrepancies in the current-loop predictions compared to real-world measurements.

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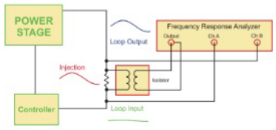
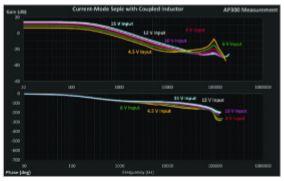
[A01] FREQUENCY RESPONSE MEASUREMENT

Frequency response measurements for a wide range of applications.



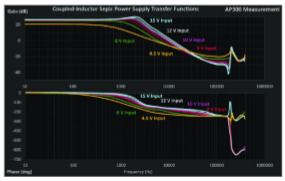
[082] SEPIC CONVERTER MEASUREMENTS - PART III CURRENT-MODE DESIGN

Measuring the Sepic converter control transfer function with current-mode control.



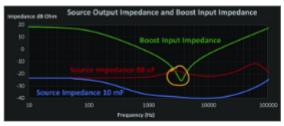
[081] SEPIC CONVERTER MEASUREMENTS - PART II COUPLED INDUCTOR DESIGN

Control measurements for the Sepic converter with coupled inductors.



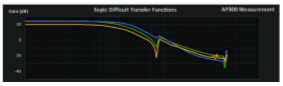
[079] INPUT IMPEDANCE INTERACTION FOR BOARD-MOUNT BOOST CONVERTER

How the point-of-load boost converter control characteristics interact strongly with the input capacitor.



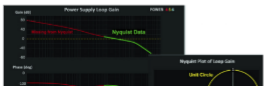
[080] SEPIC CONVERTER MEASUREMENT - PART I CONTROL TRANSFER FUNCTION

Control measurements for the Sepic converter.



[078] LOOP BODE PLOTS AND NYQUIST DIAGRAMS

Why Nyquist diagrams are not a very practical measurement.



[060] INPUT IMPEDANCE MEASUREMENTS AND FILTER INTERACTIONS PART I

The proper place to apply Middlebrook's stability criteria for input filters.

[061] INPUT IMPEDANCE MEASUREMENTS AND FILTER INTERACTIONS PART II

Measuring input filter output impedance.

3. Discrete and Continuous-Time Analysis of Current-Mode Cell

3.1 Introduction

Fig. 3.1 shows schematics of the basic two-state PWM converters operating with current-mode control. The sensed current waveform is added to an external ramp, and the peak (or valley) of the waveform is compared to a control signal to turn off (or turn on) the power switch. For the purpose of this chapter, perturbations of input and output voltage will not be considered, and only the current-mode portion of the circuit is analyzed. Fig. 3.2 shows the basic converters with the input and output voltages represented by fixed sources. All of these converters have a commonality.

When the switch is turned on, the dc voltage V_{on} is applied across the inductor. When the switch is turned off, the dc voltage V_{off} is applied across the inductor. The generic current-mode cell, shown in Fig. 3.3, therefore represents all of the converters with current-mode control. For the buck-boost converter only, the input and output voltages are equal to the on-time voltage and off-time voltages, respectively. In general, the on-time and off-time voltages are linear combinations of input and output voltages to the current-mode cell.

Analysis of this reduced block is analogous to the analysis of the PWM switch block where only the nonlinear elements of the circuit are extracted and replaced with their equivalent small-signal model. Sampled-data analysis will be used for the analysis of the current-mode block, and the results will provide a model which can be inserted into the full converter. This will be done in a later chapter, and feedforward terms will be introduced to complete the small-signal model.

It has been shown that the switch model provides accurate power stage transfer functions up to half the switching frequency. Referring to Fig. 3.1, it is apparent that the structure of the basic single-loop converter still exists when current-mode control is used. The converter is still controlled by a duty cycle input, *d,* and still produces average outputs from the states. The role of the switch model and modulator gain remain unchanged with current-mode control. The fundamental difference from average control methods, where switching frequencies are re-moved by filtering, is that current-mode control uses an instantaneous value of

the inductor current. This introduces phenomena unique to current-mode control which should be accounted for by a revised model of the current feedback.

Fig. 3.4 shows the structure of the small-signal model for the current-mode cell. The modulator gain, F_m, PWM switch model, and linear feedback gain, R_i, are the same as they would be for any average control methods. Transfer functions can be experimentally verified for these portions of the model. A gain term, $H_e(s)$, is included in the feedback loop of the inductor current. This block will be used to provide the accurate model for current-mode control where the instantaneous value of current is used for control. Another gain block, F_c, is in series with the control voltage to provide flexibility for the. model to represent different modulation schemes. For constant-frequency modulation, this gain is unity. The voltage sources of Fig. 3.3 become short circuits in the small-signal model since these sources are fixed.

The purpose of this chapter is to find the form of $H_e(s)$ and F_c for constant-frequency, constant on-time, and constant off-time control. The gain $H_e(s)$ will first be found indirectly by deriving the sampled-data expression for control-voltage-to-inductor-current with the current loop closed, for constant-frequency control. All quantities in the circuit are known except $He(s)$, which can then be solved for. It will then be shown that the simple form of $He(s)$ can be derived directly from a discrete-time system representing the modulator feedback.

Constant on-time and off-time control systems have an added complexity of a modulator gain with frequency-dependent phase characteristics. The model for these control systems will be derived by showing their similarity to constant frequency control with the appropriate external ramp in the modulator.

3.2 Discrete-Time Analysis of Closed-Loop Controller

Fig. 3.5 shows the operation of the constant-frequency, current-mode controller, with the clock initiating the on-time, and the sampled control signal ending the on-time. The sampling instant for the system is at the end of the on-time since this is when the control signal, v_c, is used. The current-ripple is not assumed to be small, but the constant input and output voltages of the current-mode cell ensure that the slopes of the current are constant. (Linear ripple.)

Fig. 3.5 shows the effect of a small perturbation $\hat{i}_L(k)$ occurring at time $t = k$, assuming that other input perturbations to the system are zero. This gives the natural response of the converter. The difference in the steady-state waveform and the perturbed waveform gives the exact small-signal perturbation shown in Fig. 3.5b. Notice that in this waveform, the sampling instant is not constant, but it is shifted by a small amount each time the the current intersects the control reference. However, this small-signal perturbation can be approximated with in-significant loss of accuracy by the waveform of Fig. 3.5c. Notice that this final

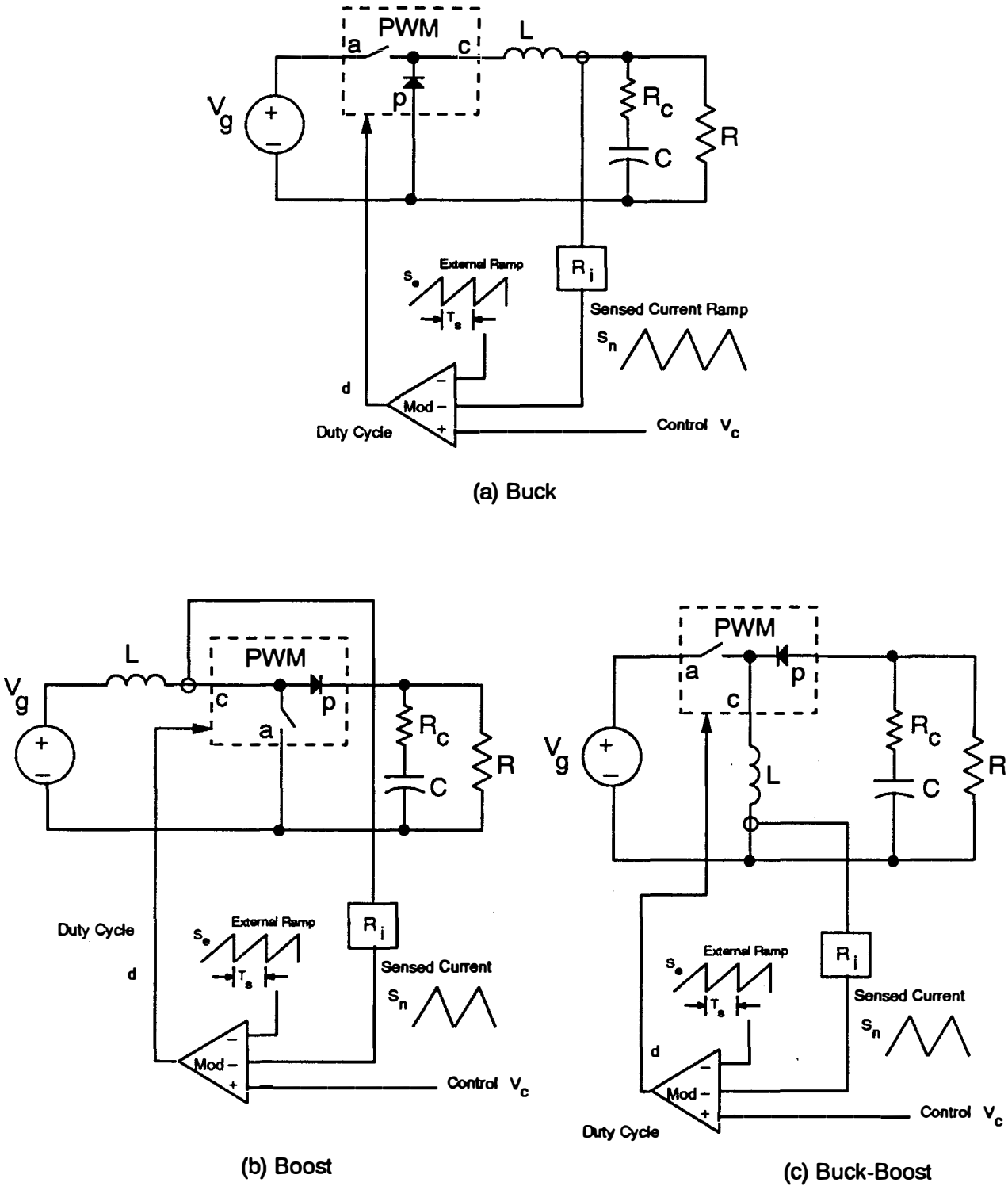


Figure 3.1. PWM Converters with Current-Mode Control: *The instantaneous value of inductor current is summed with an external ramp, and used to control the turn-on or turn-off of the switch.*

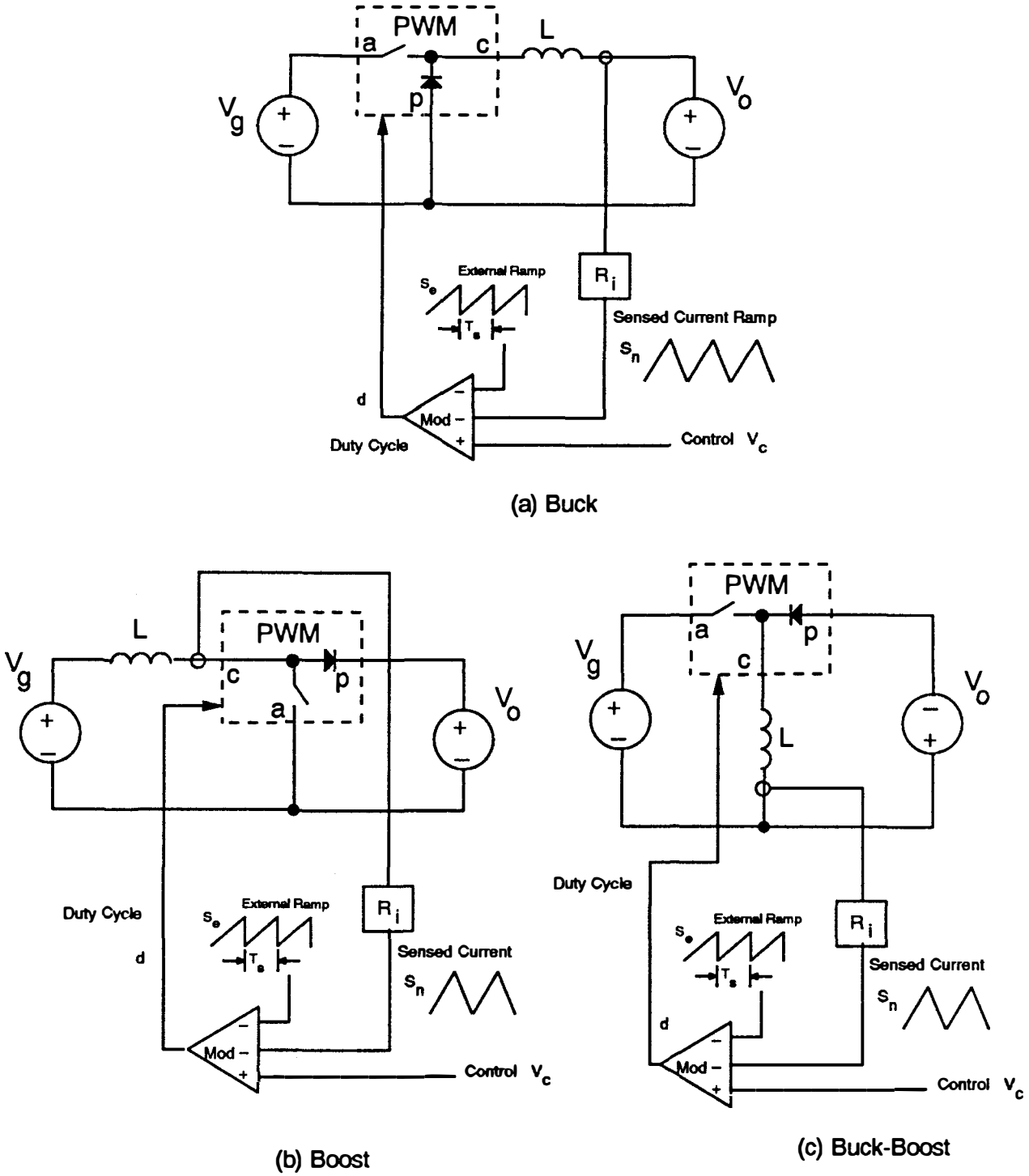


Figure 3.2. Current-Mode Converters with Fixed Input and Output Voltages: *The accurate current-mode analysis will be performed on the current-mode control converters with fixed voltages at the input and output. In a later chapter, perturbations in these voltages will be modeled to complete the analysis.*

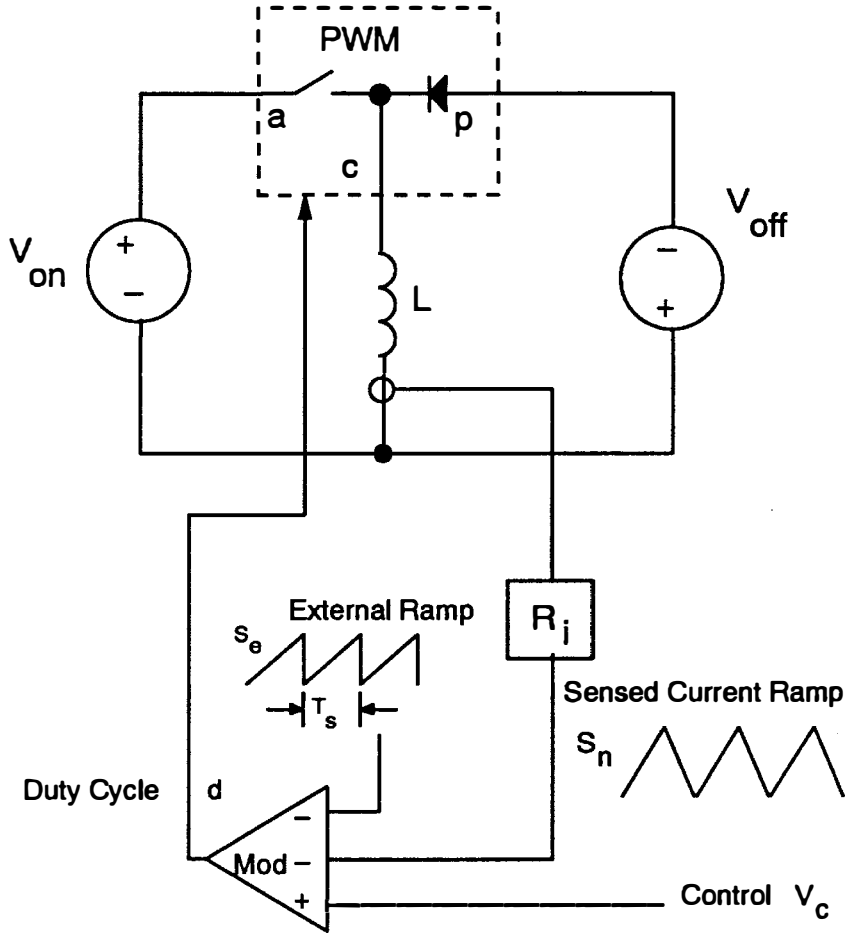


Figure 3.3. Generic Current-Mode Cell: *The generic cell represents all of the converters with current-mode feedback. The input and output voltages are now the quantities V_{on} and V_{off}, which are combinations of the input and output voltages of the different PWM converters.*

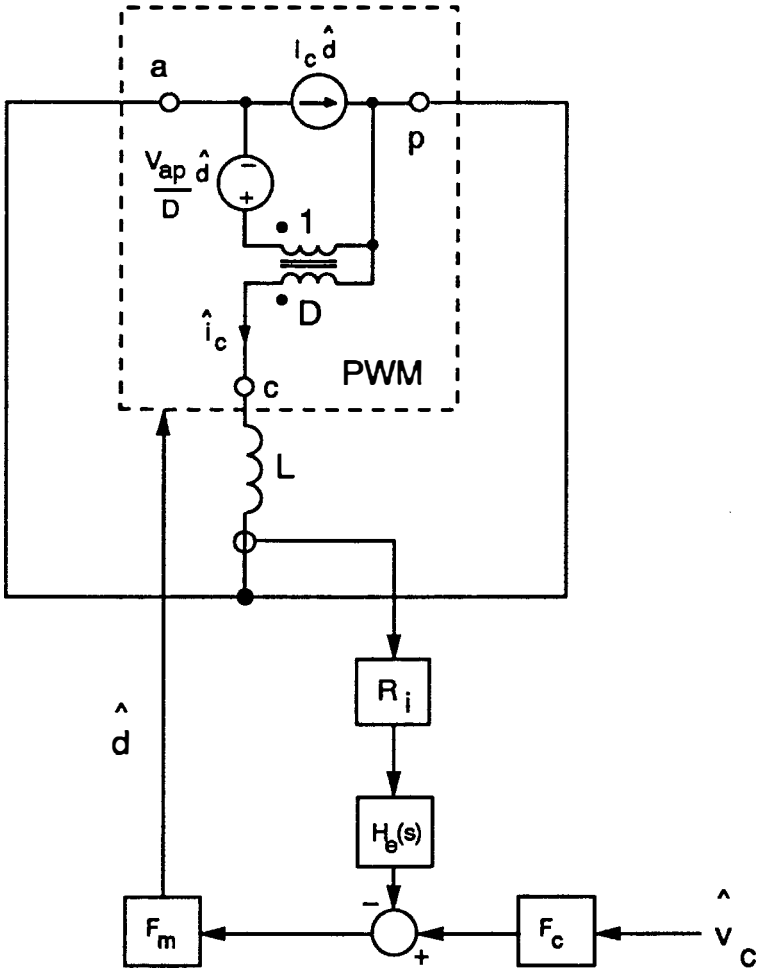


Figure 3.4. Small-Signal Model of the Current-Mode Cell with Fixed Voltages:

Gain blocks $H_e(s)$ and F_m will be used to model all of the phenomena observed for the current-mode cell of Fig. 3.3. Other quantities in the figure remain the same as predicted by average analysis.

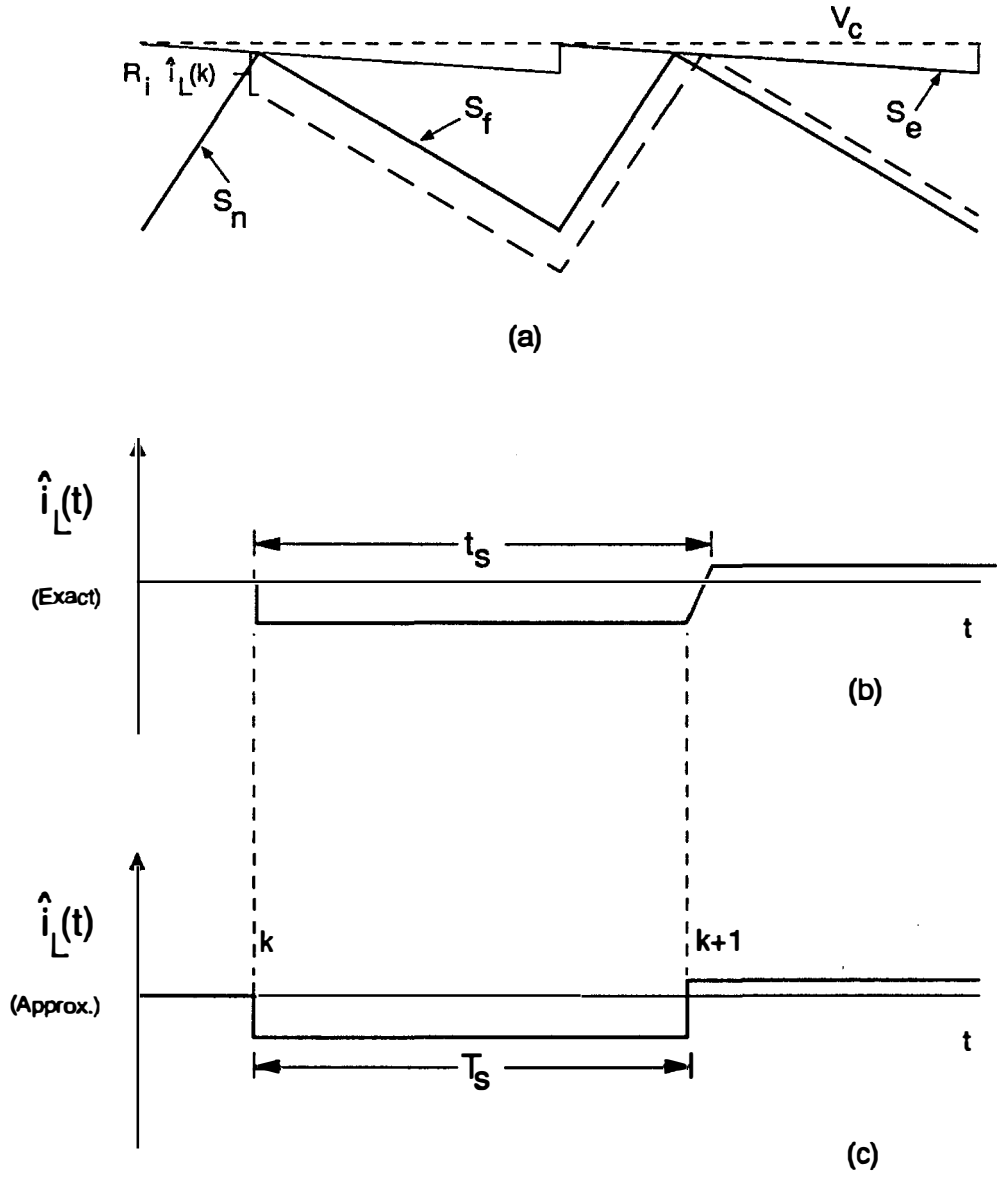


Figure 3.5. Constant-Frequency Controller with Current Perturbation:

The inductor-current waveform is controlled by a fixed reference, Ve, summed with an external ramp, S_e, Steady-state waveforms are shown with solid lines. A perturbation $\hat{i}_L(k)$ is introduced at time t = k, and the dashed lines show the propagation of the disturbance over subsequent cycles.

Fig. b shows the difference between the steady-state and the perturbed waveforms, giving the small-signal perturbation.

Fig. c shows the approximate small-signal perturbation to a pure discrete-time system.

waveform has the characteristics of a familiar first-order sample-and-hold system, with a constant sampling interval, T_S. (The original waveform had a sampling

period of $t_s = T_s + \hat{t}_s$, and the perturbation in switching times produces products of small-signal terms which can be ignored.) This is discussed in more detail in [38]. The perturbation introduced at time t = k is held constant until the next sampling instant. The difference between the exact waveform and the approximate waveform is the finite slope of the exact waveform. For small-signal per-turbations, this difference is insignificant.

The first step in analyzing such a system is to derive the discrete-time equation describing the change in inductor current from one sampling instant to the next. In the discrete-time domain, the natural response of the approximate waveform of Fig. 3.5c is given by

$$\hat{i}_L(k+1) = -\alpha \hat{i}_L(k) \tag{3.1}$$

where, with the clock initiating the on-time,

$$\alpha = \frac{S_f - S_e}{S_n + S_e} \tag{3.2}$$

and

S_n = Magnitude of slope of control ramp during on-time
S_f = Magnitude of slope of control ramp during off-time
S_e = Slope of external ramp

For the case where no external ramp is added, $S_e = 0$, and $\alpha = \frac{S_f}{S_n}$. The on- and off-time slopes are equal at a duty cycle of 0.5, and the value of α is one. At higher duty cycles than 0.5, α is greater than one. This represents a growing oscillation at the Nyquist frequency, and the current perturbation oscillates about the steady-state condition on alternate switching periods. This is the well-known subharmonic oscillation problem.

Eq. (3.1) also models a constant-frequency control scheme where the clock initiates the *off*-time, and the control voltage initiates the on-time. For this control scheme, α is given by:

$$\alpha = \frac{S_n - S_e}{S_f + S_e} \tag{3.3}$$

This type of control also demonstrates an instability, in this case occurring for duty cycles *less* than 0.5.

The forced response of the constant-frequency controller is shown in Fig. 3.6. The control voltage is perturbed by $\hat{v}_c$. Notice that the value of the control voltage at time $t = k$ produces a change in the inductor current at time $t = k$. (Note: the theory for such systems is derived for perturbations in $\hat{v}_c$ occurring at any time. However, the discrete-time equation is always derived with the perturbation at time $t = k$. A standard continuous-time transformation [35] models the continuous-time disturbance.)

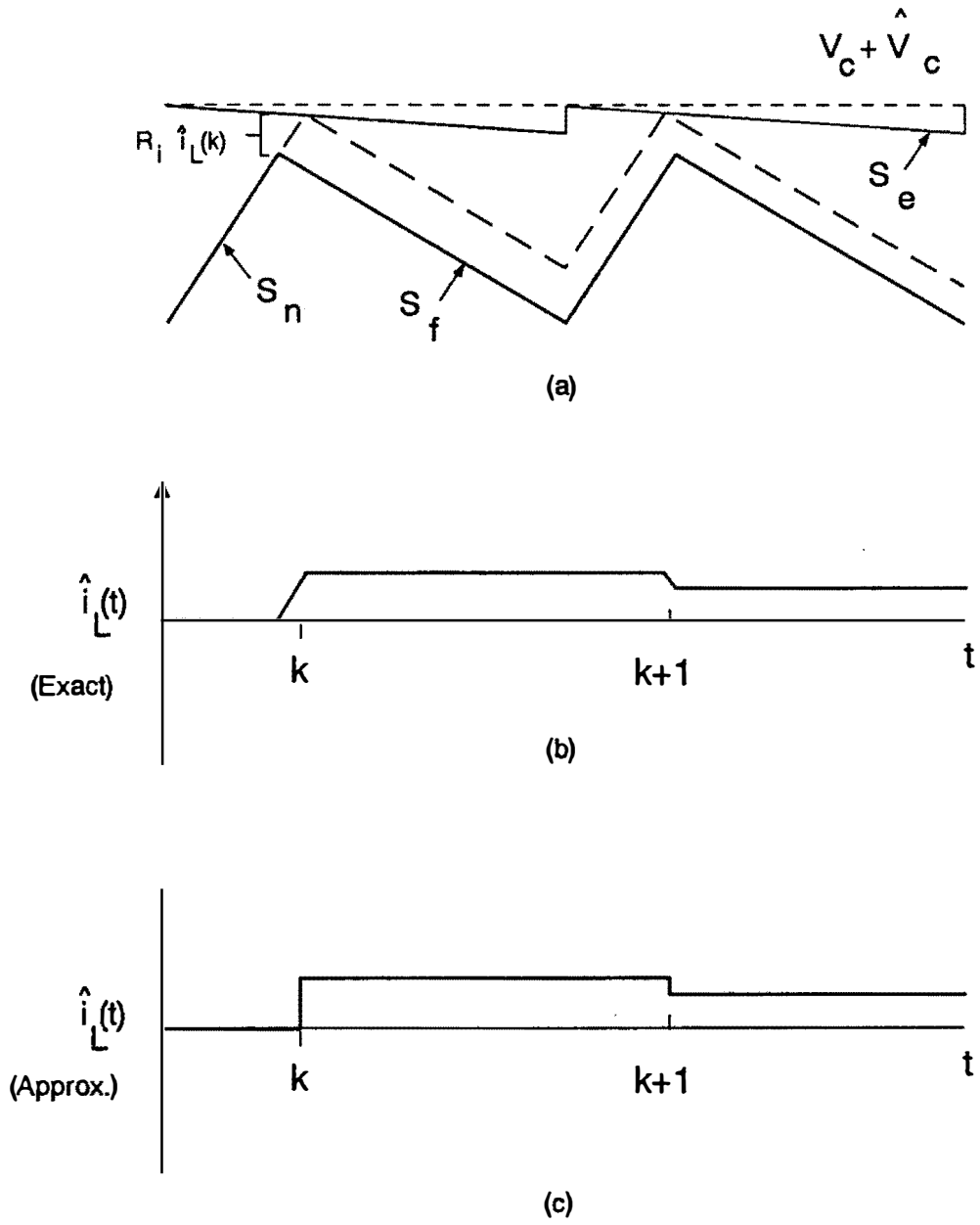


Figure 3.6. Constant Frequency Controller with Control Perturbation:

The control voltage v_C is perturbed at time t=k, resulting in an inductor current perturbation which is held constant for one cycle.

The discrete-time equation for the forced response is then given by:

$$\hat{i}_L(k+1) = \frac{1}{R_i}(1+\alpha)\hat{v}_c(k+1) \tag{3.4}$$

Combining Eqs. (3.1) and (3.4), the *complete* discrete-time response is

$$\hat{i}_L(k+1) = -\alpha \hat{i}_L(k) + \frac{1}{R_i}(1+\alpha)\hat{v}_c(k+1) \tag{3.5}$$

3.3 Continuous-Time Model of Closed-Loop Controller

Computer-controlled systems are used extensively and they have been thoroughly analyzed [35]. A computer-controlled system, which typically consists of an A-D converter, discrete-time algorithm, D-A converter, and the continuous- time system which is being controlled, is shown in Fig. 3.7. Current-mode control has a very similar structure. The control voltage is naturally sampled once in every cycle, and the perturbation in the inductor current is held constant until the next sampling instant. The 'holding' effect of the current is clearly shown in Figs. 3.5-3.6. The discrete-time process, *H(z),* is simply the z-transform of Eq. (3.5), given by:

$$H(z) = \frac{\hat{i}_L(z)}{\hat{v}_c(z)} = \frac{1}{R_i}(1+\alpha)\frac{z}{z+\alpha} \tag{3.6}$$

In order to understand and design the current-mode system properly, we now wish to transform back into the continuous-time domain. Fortunately, current-mode control is just a specific case of the general problem of computer-controlled systems as shown in Figure 3.7, and the transformation is a standard process. The transformation from the z-transform representation of Equation 3.6 to the continuous-time representation of the sample-and-hold system [35] is given by

$$F(s) = H(e^{sT_s})\frac{1}{sT_s}(1-e^{-sT_s}) \tag{3.7}$$

In other words, we substitute e^{sTs} for z in Eq 3.6, and multiply by the expression $\frac{1}{sT_s}(1-e^{-sT_s})$ as explained in [35].

For current-mode control, therefore, the exact, continuous-time, control-voltage-to-inductor-current transfer function, with the current loop closed, is

$$F(s) = \frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i}\frac{(1+\alpha)}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \tag{3.8}$$

This transfer function now predicts ***exactly*** the characteristics of the current-mode cell and it is accurate at frequencies ***well beyond the switching frequency.*** However, it is seldom used because of its complexity [28,29]. A new, approximate representation of Eq. (3.8) will be developed in the next chapter, producing very accurate results up to half the switching frequency.

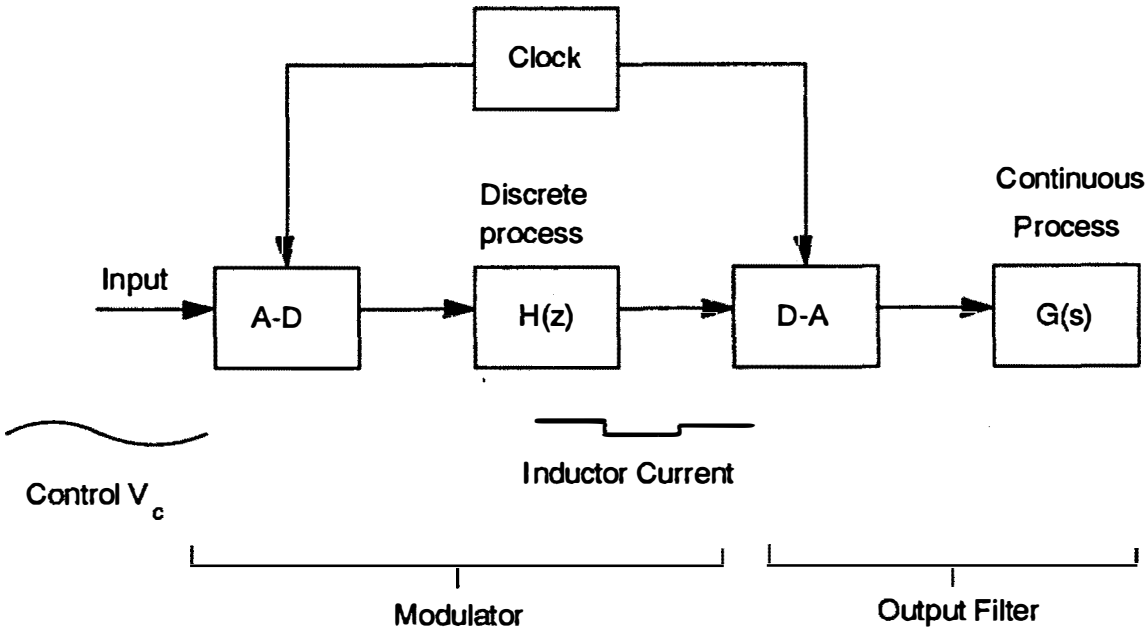


Figure 3.7. Standard Configuration of a Computer-Controlled System: *The small-signal representation of the sample-and-hold system is shown, and the analogy with current-mode control is illustrated. The analytical results for computer-controlled systems are directly applicable to current-mode control.*

3.4 Continuous-Time Model of Open-Loop Controller

The closed-loop, continuous-time model of the current-mode controller has been found. What is desired, however, is the open-loop model from which the expression for $H_e(s)$ can be found. This can be found from the control-voltage-to-inductor current transfer function found in Eq. (3.8), and from the current-mode cell model of Fig. 3.4.

The modulator gain F_m in Fig. 3.4 is the same as for voltage-mode control. For current-mode control, the ramp is formed by the sensed inductor current, and an external ramp, S_e, if constant-frequency control is used, but the modulator gain is still modeled in the same way. The modulator gain for constant-frequency control, with controlled on-time is given by the reciprocal of the height of the ramp that would be obtained if the modulator signal continued with slope $S_n + S_e$ until the end of the cycle. This is the same as the modulator gain for voltage-mode control. The fact that the ramp is derived from the current waveforms is accounted for by feedback loop of the current, and the modulator mechanism is unchanged.
The gain is therefore:

$$F_m = \frac{1}{(S_n + S_e)T_s} \tag{3.9}$$

This gain differs from the models [16,18] which had the problem of predicting a current loop crossover in excess of half the switching frequency. *(See Chapter 3 Appendix for further discussion of correct choice of modulator gain.)*

The modulator gain for constant-frequency control, with the clock initiating the *off*-time

$$F_m = \frac{1}{(S_f + S_e)T_s} \tag{3.10}$$

For constant-frequency control with a naturally-sampled control signal there is no frequency dependence of modulator gain or phase [36], and the gain block $F_c = 1$.

The duty-cycle-to-inductor-current transfer function can be easily derived from Fig. 3.4 to be

$$F_i(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{ap}}{sL} \tag{3.11}$$

Recognizing that $V_{ap} = V_{ac} + V_{cp}$ and that $S_n = \frac{R_i V_{ac}}{L}$ and $S_f = \frac{R_i V_{cp}}{L}$, this expression can be rewritten in terms of the control signal slopes:

$$F_i(s) = \frac{1}{R_i}\frac{S_n + S_f}{s} \tag{3.12}$$

The product of the modulator gain F_m and the current gain $F_i(s)$ is then a single expression for all converters:

$$F_m F_i(s) = \frac{1}{R_i}\frac{1+\alpha}{sT_s} \tag{3.13}$$

The open-loop gain term $H_e(s)$ can now be found by equating the closed-loop expression of Eq. 3.8 with the forward gain of Fig. 3.4 divided by one plus the current-loop gain:

$$\frac{1}{R_i}\frac{1+\alpha}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha}=\frac{F_mF_i(s)}{1+F_mF_i(s)R_iH_e(s)} \tag{3.14}$$

Substituting Eq. 3.13 for $F_mF_i(s)$, the very simple result is obtained

$$H_e(s)=\frac{sT_s}{e^{sT_s}-1} \tag{3.15}$$

This result was obtained by Brown [29] for the buck converter operating in constant-frequency mode. In this chapter, the analysis is simplified and generalized for ***all*** converters containing the current-mode cell.

The expression for $H_e(s)$ has been derived here for the general current-mode control cell, and is not specific to one converter. It will be shown later that it can also be extended to constant on-time and constant off-time control schemes. As mentioned in [29], the form of $H_e(s)$ is difficult to work with when designing a control system. In the next chapter, a simple second-order representation of $H_e(s)$ will be given, capable of accurately predicting current-mode phenomena up to half the switching frequency. This also gives a simple second-order function for the closed-loop, control-to-inductor-current transfer function which will prove to be the most useful for design purposes.

3.5 Discrete-Time Analysis of Open-Loop Controller

The simple form of $H_e(s)$, and the fact that it is the same for all forms of current-mode control and invariant with all power stage parameters except switching frequency, suggest that it could be derived directly with very simple arguments. Consider the modulator function shown in Fig. 3.8, with the control voltage v_c kept constant. A perturbation $i_L(k)$ is introduced at time $t = \mathrm{k}$. This perturbation affects the next switching instant, causing a perturbation in the switching time $t(k + 1)$ where

$$\hat{i}_L(k) = -(S_n + S_e)\hat{t}(k+1) \tag{3.16}$$

for constant-frequency control, with a clock initiating the on-time. The perturbation in duty cycle is then related to the perturbed current by

$$\hat{i}_L(k) = -\frac{1}{F_m}\hat{d}(k+1) \tag{3.17}$$

Eq. (3.17) is intentionally written in this form, with the duty cycle on the right-hand side, and with the change in current at time $t = k$ dependent upon the duty cycle at time $t = \mathrm{k} + 1$. It has been shown that the variable $\hat{i}_L(k)$ is the 'held' variable of the system, remaining constant from time $t = k$ to time $t = k + 1$. The duty cycle $\hat{d}$ is the sampled input, being just a scalar multiple of the control voltage, v_c, and the current feedback signal, i_L. The correct z-transform representation of this sampled-data subsystem is then given by the equation

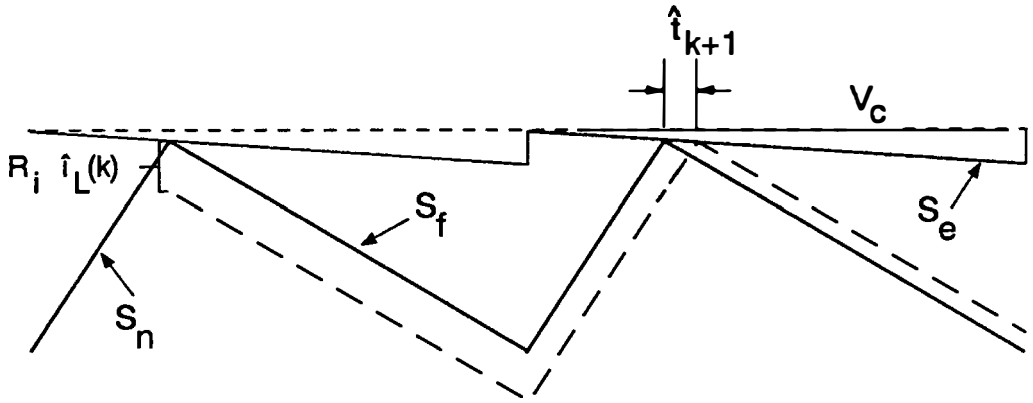


Figure 3.8. Current-Mode Control Modulator with Perturbation in Current: *The control voltage v_c is constant, and a perturbation in $\hat{i}_L$ is introduced at time $t = k$, causing subsequent change in duty cycle $\hat{d}(k+1)$.*

$$\hat{i}_L(z) = -\frac{1}{F_m} z\hat{d}(z) \tag{3.18}$$

The corresponding sampled continuous-time model is

$$\begin{aligned}\hat{i}_L(s) &= -\frac{1}{F_m} e^{sT_s} \frac{1-e^{-sT_s}}{sT_s} \hat{d}(s) \\ &= -\frac{1}{F_m} \frac{e^{sT_s}-1}{sT_s} \hat{d}(s)\end{aligned} \tag{3.19}$$

The gain block $H_e(s)$ from Fig. 3.4 and from Eq. (3.19) is then

$$\begin{aligned}H_e(s) &= -\frac{1}{F_m} \frac{\hat{d}(s)}{\hat{i}_L(s)} \\ &= \frac{sT_s}{e^{sT_s}-1}\end{aligned} \tag{3.20}$$

Notice that gain terms containing R_i appear in the expression for the current transfer function, and the modulator gain, and these terms are cancelled. This is the same result that was obtained indirectly in the previous part of this chapter, confirming the analysis approach.

3.6 Extension of Modeling for Constant On-Time or Constant Off-Time Control

Constant on-time or constant off-time modulators are sometimes used instead of constant-frequency modulators [37]. These control schemes can offer advantages of low audio susceptibility, ease of implementation, or lower power stage weight. Also, converters with this modulation do not exhibit the subharmonic oscillation problem associated with constant-frequency control. The most commonly-used scheme is the constant off-time modulator, since the inductor current is easily sensed with a current transformer in series with the power switch.

There are many different schemes which can be used to provide constant on- or off-time modulation. Fig. 3.9 shows the most commonly-used scheme for generating constant off-time control. A PWM ramp signal (the inductor current signal for current-mode control) is started when the power switch is turned on, and this provides the turn-off command when the ramp intersects the modulated control signal, v_c. This scheme gives an on-time pulse of varying width. The falling edge of the PWM output pulse starts a timer which provides the fixed off-time signal. The falling edge of the timer triggers the turn-on of the power switch. An external ramp is rarely used for constant off-time modulation, and it is not considered here. The constant on-time controller is the dual control scheme of constant off-time. A timer provides a fixed on-time, and the current ramp, or PWM ramp,

is used to turn the switch on. In this case, the valley of the inductor current not the peak of the current, is used to control the turn on.

It is easy to show that the average gain of the constant off-time modulator is given by

$$F_m = \frac{D'}{S_n T_s} \tag{3.21}$$

Notice that this is the same gain as that for the constant-frequency modulator, multiplied by D'.

The constant off-time modulator described above shows an interesting characteristic. Unlike the naturally-sampled constant-frequency modulator which has flat gain and phase [36], the constant off-time modulator exhibits a phase-lead characteristic which increases linearly with duty cycle and with frequency. Fig. 3.10 shows the measured phase characteristics of the constant off-time modulator for different duty cycles, and compares this with the constant-frequency modulator with a duty cycle of 0.45.

It is important to emphasize that the exact mechanism for the generation of the constant off-time pulse is critical in predicting the small-signal characteristics of the modulator. There are many different timing mechanisms for the generation of this signal, and a few of these are described in [8,9]. It is also shown in these references that one interesting modulator actually can generate ninety degrees of

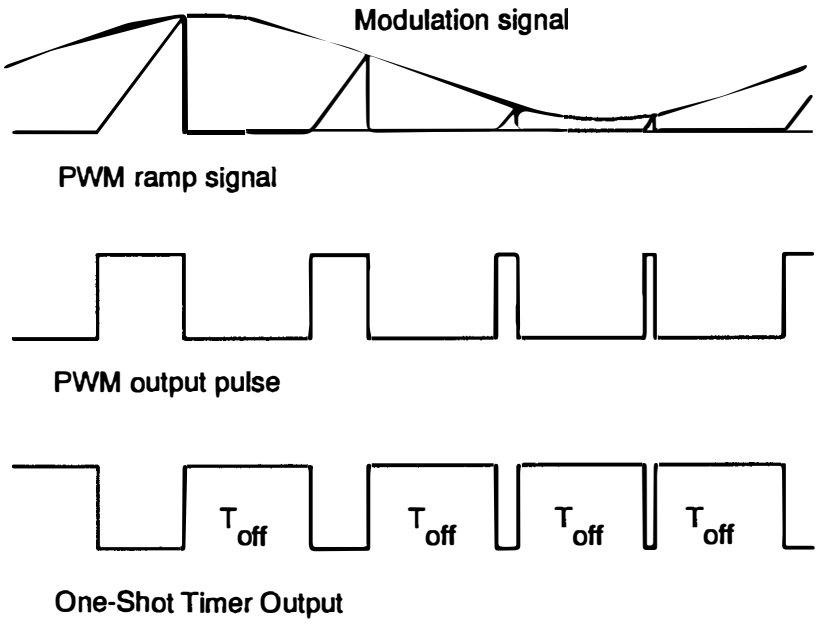


Figure 3.9. Constant Off-Time Modulator Waveforms:

A timer is started when the switch is turned off to provide a constant off-time pulse. A ramp is initiated when the switch is turned on, and the intersection of the ramp with the modulation signal is used to provide the signal to turn the switch off.

phase ***lead*** at all frequencies. The phase lead in general for these schemes is produced by an effective differentiation of the input signal by the modulator.

The constant off-time modulator with a duty cycle of only 0.1 gives a small phase lead of only 10 degrees at half the switching frequency. However, this phase lead increases to 45 degrees at a duty cycle of 0.5, and to 90 degrees at a duty cycle of 1. The gain of the modulator, not shown in Fig. 3.10, also shows an increase at frequencies approaching half the switching frequency at higher duty cycles, but this effect is not modeled. This gain change is produced by sidebands of information appearing at higher duty cycles. Exact analysis of this effect [8,9] is possible, but any incremental enhancement to the accuracy of the new current-mode model is insignificant.

For constant-frequency control, the gain block, F_c, of Fig. 3.4 was unity since there was no frequency dependence in the modulator gain. For variable-frequency control, this gain term is used to account for the phase dependency of the modulator, and it will be shown that the model of Fig. 3.4 is equally valid for variable frequency control with the appropriate values of F_c. For constant ***off***-time, it is given by

$$F_c = e^{sDT_s/2} \tag{3.22}$$

For constant ***on***-time it is given by

$$F_c = e^{sD'T_s/2} \tag{3.23}$$

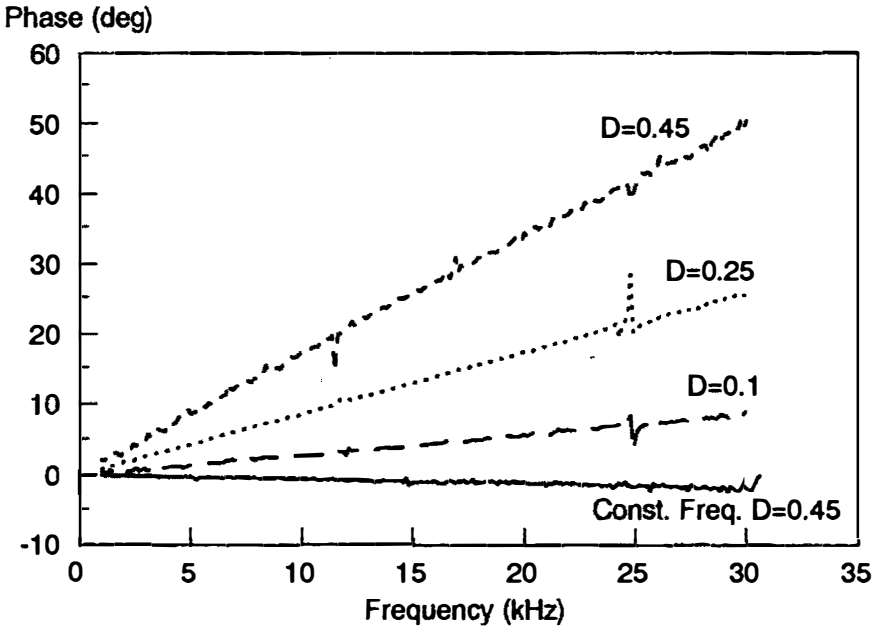


Figure 3.10. Constant Off-Time Modulator Phase Measurement:

The constant off-time modulator shows a linear phase lead, the slope of which depends on the duty cycle. The constant on-time modulator also shows a phase lead, the slope of which depends upon the complement of the duty cycle, D' = 1-D.

These terms are approximate: at frequencies close to the switching rate, an increase in gain is observed. However, these approximations are adequate for purposes of the current-mode control model. Notice that the product of the gains $F_c F_m$ gives the complete modulator gain for voltage-mode control.

The model for constant on-time and constant off-time control is best derived by comparing the system response with that of constant-frequency control with an appropriate external ramp. Fig. 3.11a shows the control waveforms for a constant-frequency converter with an external ramp equal to the off-time slope of the sensed current waveform. A perturbation in the current at time $t = k$ is exactly damped out in one switching cycle. After the next sampling instant, the inductor current returns to its previous trajectory. This system corresponds to a 'dead-beat' control scheme. The expressions of Eqs. (3.1) and (3.5) are valid with a value of $\alpha = 0$. Referring to Eq. (3.6), the z-transform equation then has a pole at the origin which corresponds to dead-beat control. The modulator gain of the constant-frequency control, given in Eq. (3.9), for an external ramp equal to the off-slope of the current signal, reduces to:

$$F_m = \frac{D'}{S_n T_s} \tag{3.24}$$

This is the same modulator gain as that for the constant off-time control, given in Eq. (3.21).

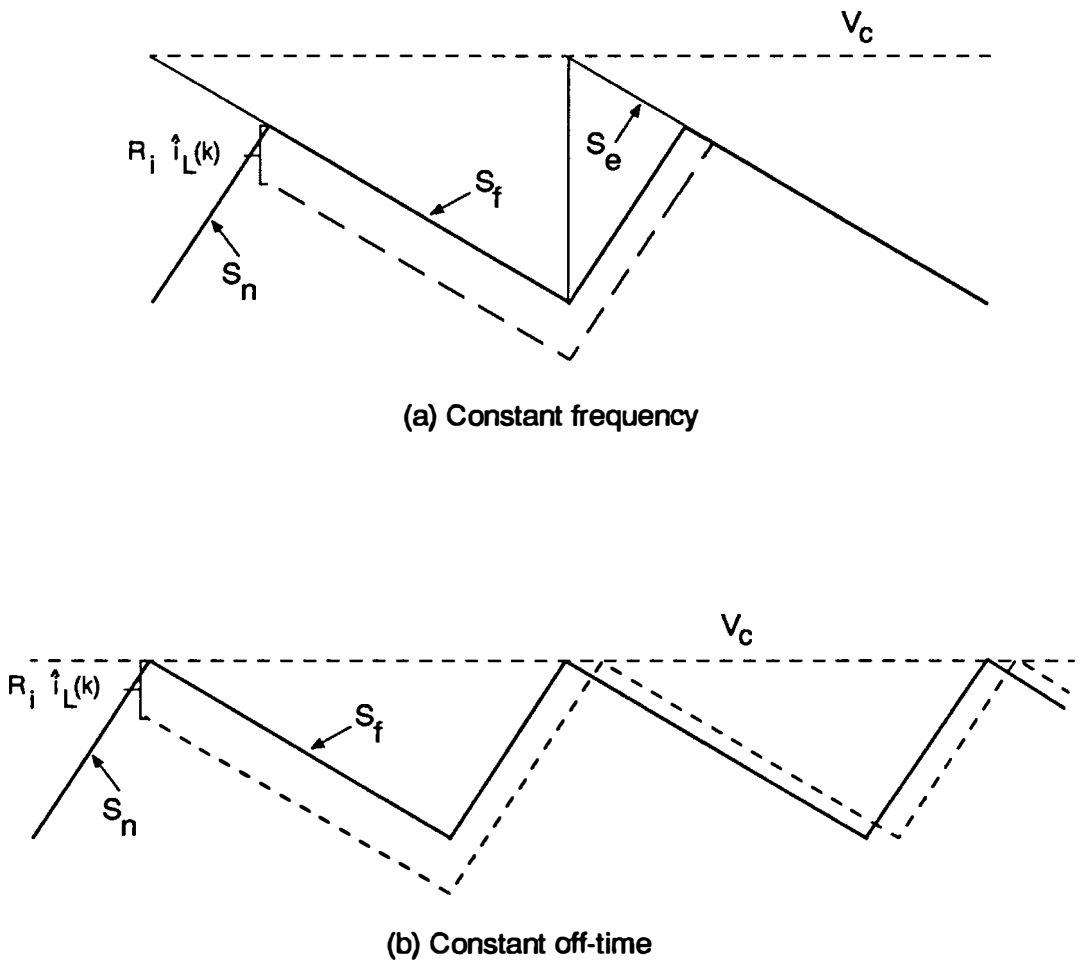


Figure 3.11. Comparison of Constant-Frequency and Constant Off-Time Control:

The natural response of the current-mode controller for constant frequency with external ramp equal to the off slope is shown with constant off-time control. Both systems exhibit 'dead-beat' control characteristics.

Fig. 3.11b shows the natural response of the constant off-time controller, with no external ramp. Like the constant-frequency controller described above, the perturbation from steady-state is exactly damped out after the next sampling instant. The constant off-time modulator gain, given in Eq. (3.21) is the same as that for the constant-frequency control with the external ramp. It is important to note that the constant off-time system perturbations are compared to the steady-state waveforms shifted in time to correspond to the new frequency. It was shown in [38] that the small time shift is a second-order effect which can be ignored. The current-loop dynamics of the constant off-time (and constant on-time) system are the same as those for the constant-frequency control with the external ramp equal to the off-time slope. The model of the current loop in Fig. 3.4 is valid for each of these forms of current-mode control, with the same invariant value of the sampling gain, $H_e(s)$, as was found previously. The phase lead term, F_c, does not appear inside the current loop gain.

An important difference exists for constant on-time and constant off-time controls for the control-to-output response. Notice that the model of Fig. 3.4 contains the gain block $F_c(s)$ which introduces a phase lead in the system. In the absence of current feedback ($R_i = 0$), the forward gain of the converter from control voltage to the output voltage is simply the modulator gain for voltage-mode control, $F_c F_m$, times the power stage gain from duty cycle to output voltage. The control-to-output characteristic for current-mode control must also show this phase-lead characteristic for the model of Fig. 3.4 to be correct for variable-frequency control.

Fig. 3.12a shows the response of the constant-frequency control, with $S_e = S_f$ with a control input perturbation, over several cycles of operation. The waveforms of the small-signal perturbations show the inductor current signal changing in discrete steps (if the transition slopes are ignored), and tracking the control signal exactly. Again, this is a feature of dead-beat control systems. Fig. 3.12b shows the response of the constant off-time converter to the same input perturbation. In this case, the small-signal perturbation is slightly different. Due to the nature of the control, the perturbations in current appear as discrete pulses that terminate before the end of the switching cycle. It is important to note that the ***average*** magnitude of the perturbation over the full cycle is equal to the perturbation of the constant-frequency control system.

The variations in the small-signal perturbations provide a phase lead relative to that of the constant-frequency system. The width of the pulse with the constant off-time control is given by

$$P_w = D'T_s \tag{3.25}$$

At a duty cycle of zero, the pulse width is equal to that of the constant frequency control system, and there is no phase lead. This situation is shown in Fig. 3.13a. At close to unity duty cycle, the pulse becomes an impulse function, and the information carried leads that of constant-frequency system by half the switching period. At half the switching frequency, this corresponds to a 90 degree phase lead, which is predicted by Eq. (3.22).

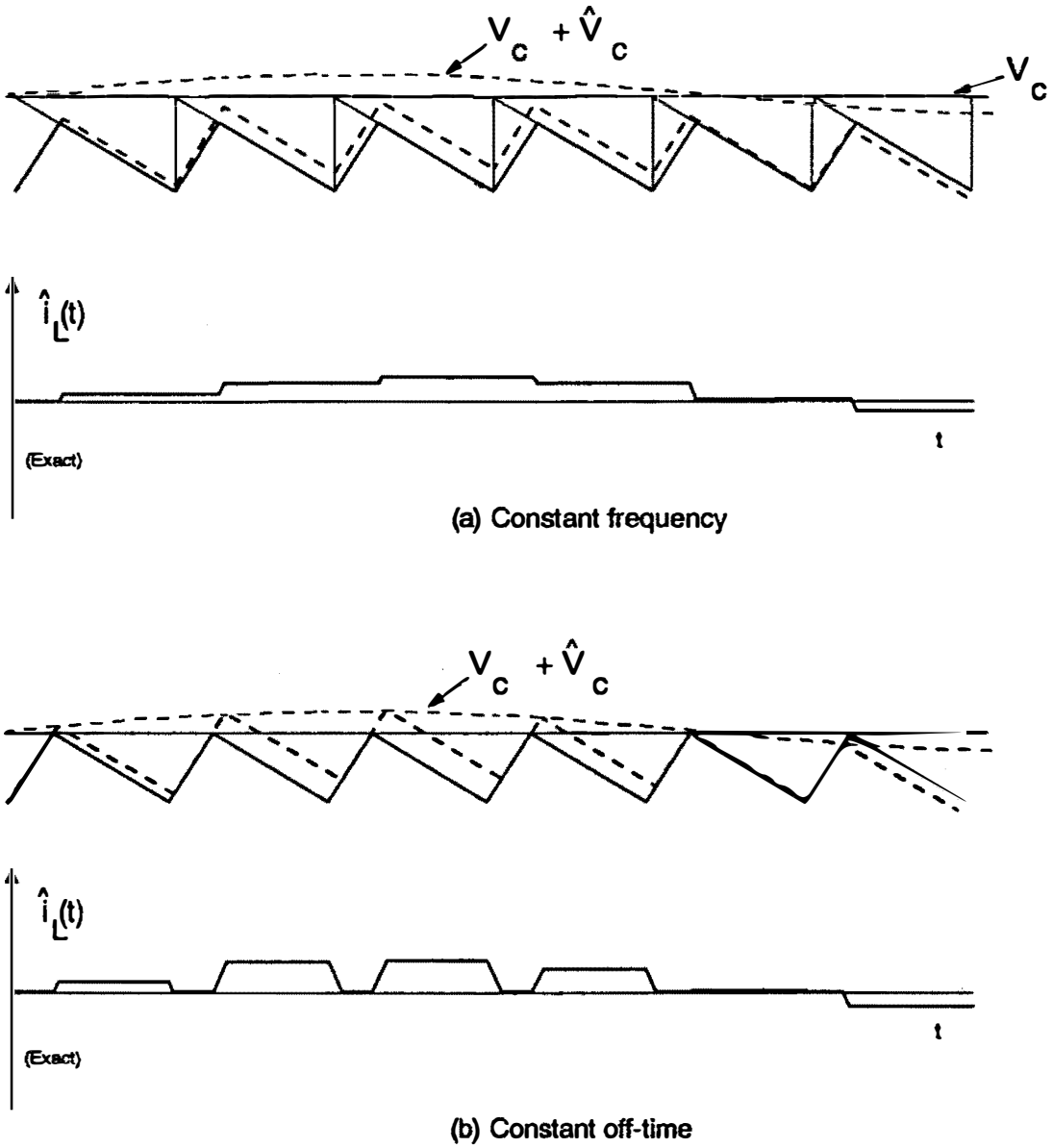


Figure 3.12. Comparison of Constant-Frequency and Constant Off-Time Control:

The forced response of the current-mode controller for constant frequency with external ramp equal to the off slope is shown with constant off-time control. The off-time response carries the same average information in shorter pulses of current perturbations.

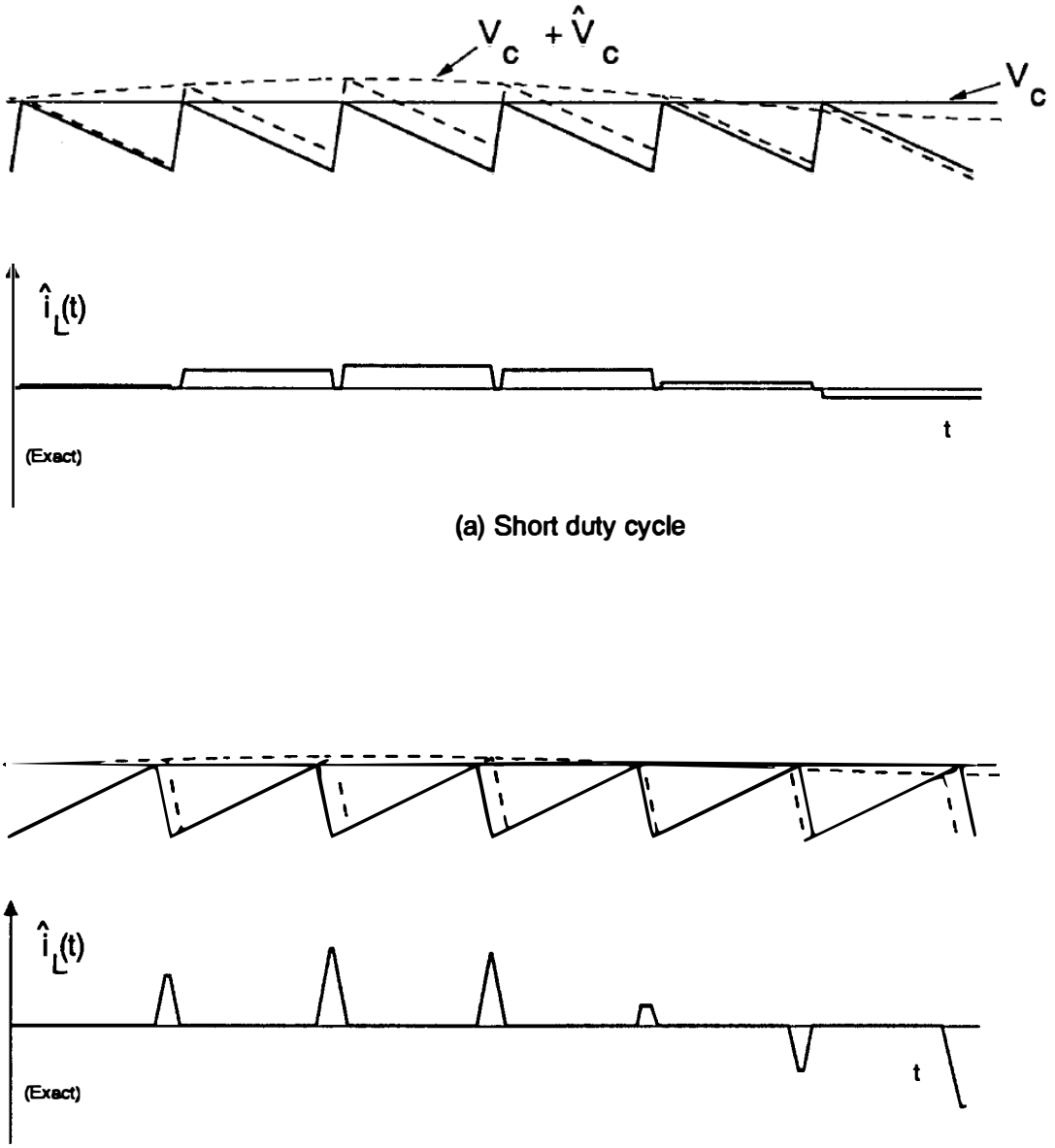


Figure 3.13. Constant Off-Time Responses at Different Duty Cycles: *At duty cycles close to zero, the response of the constant-frequency and constant off-time controls are practically identical. At duty cycles close to one, almost 90 degrees phase lead occurs at half the switching frequency with constant off-time control, due to the shorter pulses of information.*

Fig. 3.14 show the perturbation waveforms of Fig. 3.13 more clearly, together with the modulation information carried by the pulses. The shorter pulses at duty cycles close to unity advance the information relative to that of the short duty-cycle system, by half the switching period. An alternative way of looking at this is that the duty cycle close to unity samples the input modulation signal with impulse functions (or an approximation thereof). Impulse sampling does not introduce a phase delay. However, the step-function sampling obtained with the duty-cycle close to zero produces a phase delay equal to half the switching period, as is well known from communication theory [8,9].

The constant off-time control scheme, therefore, shows exactly the same response as the constant-frequency control scheme, when an external ramp equal to the off-time slope is used, with the exception of a phase-lead of the inductor current information, predicted by the value of F_c given in Eqs. (3.22-3.23). The constant off-time and constant on-time current-mode schemes, therefore, are accurately modeled by the small-signal model of Fig. 3.4.

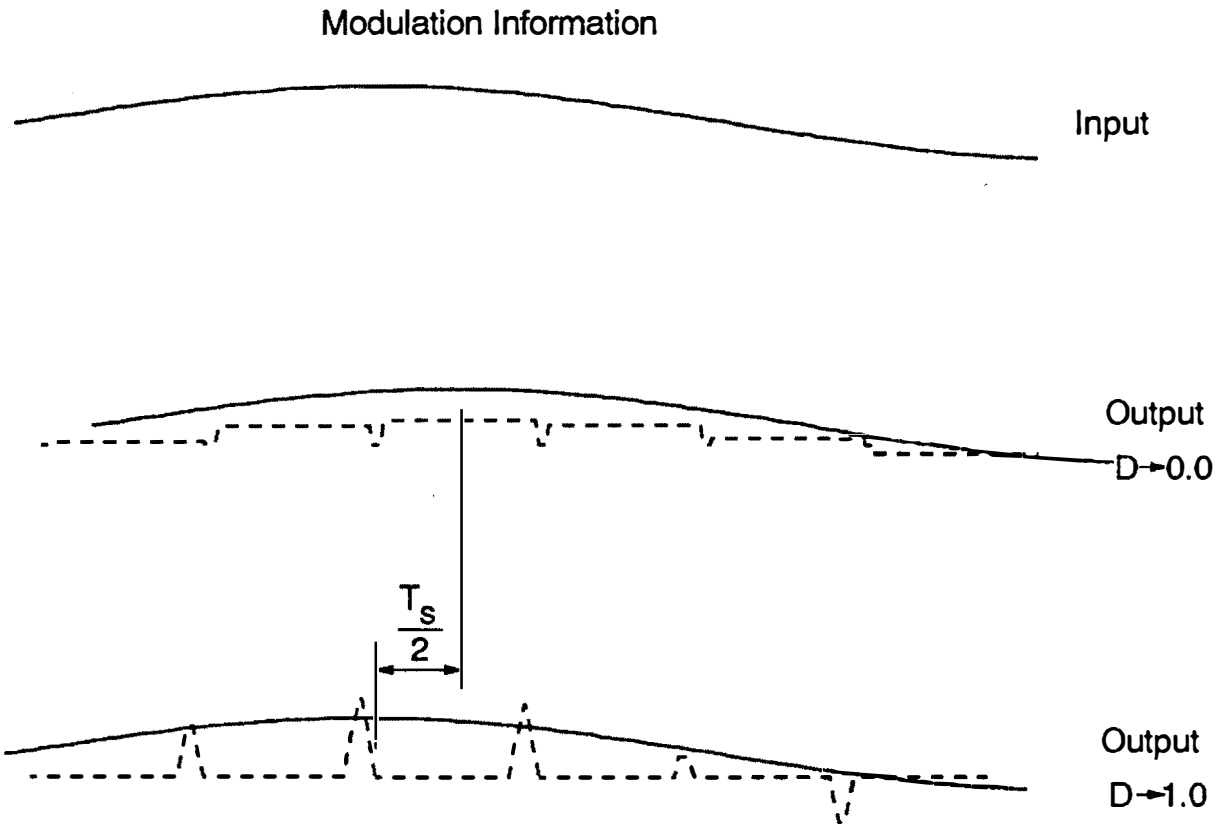


Figure 3.14. Modulation Information Carried by Constant Off-Time Modulator:

At duty cycles close to unity, modulation-frequency information carried by the perturbations in the inductor current is time-shifted by almost half the switching period relative to that carried by the modulator at close to zero duty cycle.

3.7 Conclusions

Several important results were derived in this chapter for the four common forms of current-mode control. Firstly, a generic current-mode cell was derived for all PWM converters using current-mode control. The discrete-time response of the closed-loop control-to-inductor-current for constant-frequency control of the current-mode cell was found to be

$$\hat{i}_L(k+1) = -\alpha \hat{i}_L(k) + \frac{1}{R_i}(1+\alpha)\hat{v}_c(k+1) \tag{3.26}$$

The continuous-time representation of the system, derived from standard results for sample-and-hold systems, is

$$F(s) = \frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i}\frac{(1+\alpha)}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha} \tag{3.27}$$

This equation was used to derive the open-loop gain block $H_e(s)$ shown in Fig. 3.4. This block was found to have a common form for all converters and all four forms of current-mode control discussed in this dissertation:

$$H_e(s) = \frac{sT_s}{e^{sT_s}-1} \tag{3.28}$$

This high-frequency gain block is sufficient to characterize the crucial characteristics of current-mode control with constant frequency operation. Notice that the correct form of $H_e(s)$ can *only* be found if the proper version of the modulator gain is used.

For constant on-time and off-time control schemes, it was found that a phase-dependent term, F_c , added to the model of Fig. 3.4, provides a general model for all control schemes for the current-mode cell. (The gain F_c is unity for constant-frequency control.)

Chapter 3 Appendix
Resolving the Modulator Gain Issue

At the time this dissertation was first written, the importance of the modulator gain was not stressed. It did not seem necessary to emphasize that other researchers had made errors of any kind, it was more important to move on with a correct model for the future. However, since the publication of the dissertation, many more researchers have repeated errors and assumptions in their analysis, and erroneous modulator gains have reappeared in the literature.

This confusion needs to be cleared up - you cannot have different models simultaneously predicting different results. This is confusing for anyone entering the field and reading the literature.

The earliest attempts at modeling current-mode control were performed at Virginia Tech by Dr. Fred Lee, while working on NASA contracts. He used describing function techniques for find the perturbation in the duty cycle of the modulator with respect to the perturbations in the average current in the inductor. The resulting expression for the gain F_m is then found to be:

Lee's expression

$$F_m = \frac{2}{(S_n - S_f + 2S_e)T_s} \qquad \text{(Eq. A3.1)}$$

Although the work by Lee provided an excellent framework for designing current-mode systems, it did not get widespread use. It was performed on a system that built a simple and effective observer for current-mode control, and working engineers wrestled with the applicability of the concept.

Current-mode became widely popular after the concept of current-injection straight into the PWM comparator was introduced. Middlebrook [18] provided analysis in 1985 for current-injection control and his work was immediately popular with industry. He used easy-to-understand waveform analysis to arrive at his version of F_m which was found to be:

Middlebrook's expression

$$F_m = \frac{2}{(S_n + 2S_e)T_s} \qquad \text{Eq. A3.2}$$

The original paper by Middlebrook [18] is a standard reference for almost all papers on current-mode control

Other researchers used a different expression for the modulator gain. Vince Bello was a working engineer in industry who produced a lot of circuit simulation models for Spice. He observed that the comparator for current-mode control was the same as for voltage-mode control, hence the gain should be the same - the recipricol of the ramp height. In the case of current-mode, the ramp is formed by the sensed current slope, S_n , and the added slope S_e.

Brown and Bello's expression $$F_m = \frac{1}{(S_n + S_e)T_s}$$ (Eq A3.3)

Art Brown, a PhD student at Caltech (also Middlebrook's student) agreed with Bello in his foundational work which applied discrete-time and sampled-data modeling to current-mode control [28,29].

So here you have a very interesting situation in 1986. Three highly-renowned PhD researchers have three very different gains for a simple modulator. Furthermore, Middlebrook's name was on his 1986 paper, and also on Brown's paper both having different expressions. Needless to say, this has led to much confusion amongst students and working engineers. Which result should you use?

Here is another baffling part of the puzzle. If you read through the papers from Lee, Brown, Bello, and Middlebrook, you will not be able to identify an analytical error, however hard you try.

Figure A3.1 shows the resulting current-loop gains with these different predictions for the modulator gain. Both Lee and Middlebrook predict crossover frequencies for the current loop in excess of half the switching frequency. Since current-mode control is a sampled-data system, Nyquist would predict that such a high crossover is actually impossible.

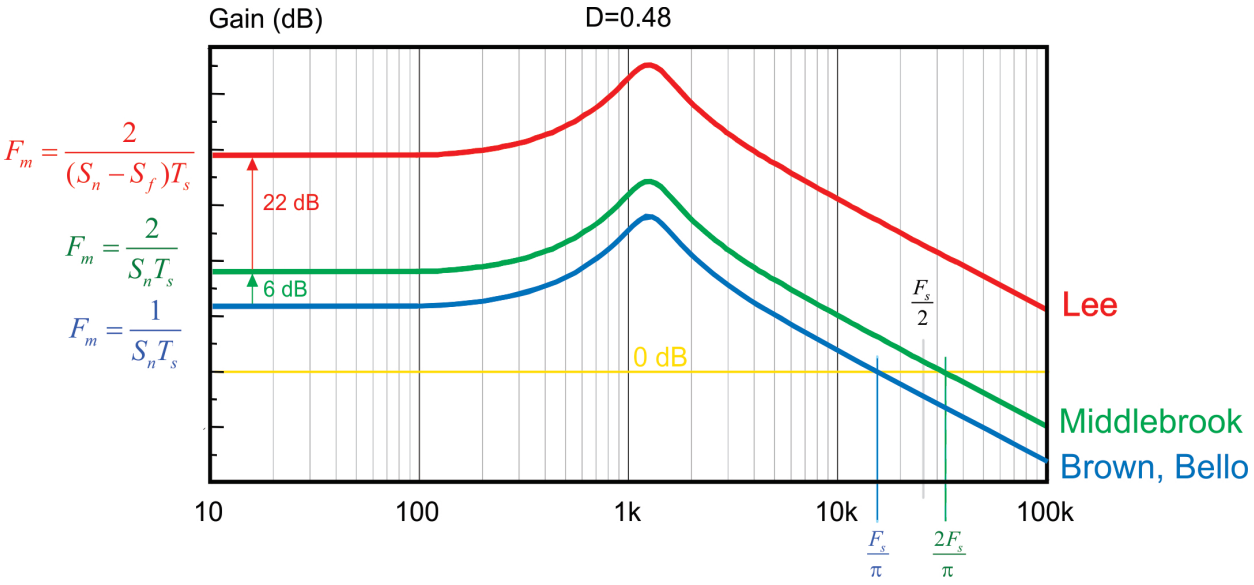


Figure A3.1 Current-Mode Loop Gains from Lee, Middlebrook, and Bello (Brown):

Plots are shown for a duty cycle very close to 50%. The gain predicted by Lee is very large if no ramp is added since the on- and off-time slopes are very close in magnitude. Middlebrook's result is lower, but still 6 dB higher than predicted by Bello and Brown.

Both Lee and Middlebrook predict a crossover frequency above half the switching frequency - an impossible result according to Nyquist.

How could these discrepancies exist without being resolved for many years? The answer to this depends on several coincident factors that obscured the modulator gain from being a key parameter in the past:

(1) When Middlebrook wrote his paper in 1986, he did not explicitly pull out the parameter F_m.

(2) Middlebrook was strongly opposed to the philosophy of defining and measuring a current loop at all. He believed that this was the wrong approach to designing current-mode systems. His view of this was supported by the fact that it is very difficult to measure the current loop with conventional techniques, and this is rarely done.

(3) Lee, who started on current-mode analysis earlier, worked with discrete circuit implementations of current mode control since control chips for current-mode were not available at the time. His observor implementation, used by NASA, *did* allow current-loop measurement. However, due to the discrete implementation, the constant-frequency version of current-mode was regarded as too troublesome because of its instability. Implementations in hardware were usually done for constant on-time and constant off-time control where the large variation in modulator gain does not exist.

(4) Most people reading Middlebrook's work would not have been aware of Lee's work, and would be unlikely to extract and compare modulator gains.

(5) Nobody in industry was likely to measure the current loop, it is too hard to do in hardware.

(6) If researchers did measure a current loop, it was with a compensating ramp added, and this reduces discrepancies.

Current-Loop Measurements

After months of reading and comparing papers, there was no resolution of this issue in sight. Finally, late one evening, I decided to go to the lab to settle the issue once and for all with some hardware measurements. My plan was to add varying amounts of compensating ramp to a current-injection system to see which equation fit the measurements the best. Since I was a student of Dr. Lee's, I was pretty sure what I was going to see - I expected the modulator gain to be very large as 50% duty cycle was approached with no ramp added, as predicted by Equation A3.1.

However this didn't happen. Figure A3.2 show the original current loop measurements recorded with an HP4194A analyer on a buck converter running with current mode control. Measured current-loop gains made with a digital modulator.

The black traces are for measurements with differing amounts of compensating ramp. The top black measurement is with no external ramp, and this agrees ***exactly*** with the predictions of Bello and Brown.

At no time did any of the measurements exceed half the switching frequency, consistent with Nyquist predictions for sampled-data loops.

Modulator gains predicted by Middlebrook and Lee are shown to be wrong. There is no avoiding this fact. Yet, despite the publication of this set of measurements, researchers persist in deriving models with varying modulator gains.

There is only one correct modulator gain, the one that is verified by measurements in the lab. Make sure you use Eq. A3.3 in your models.

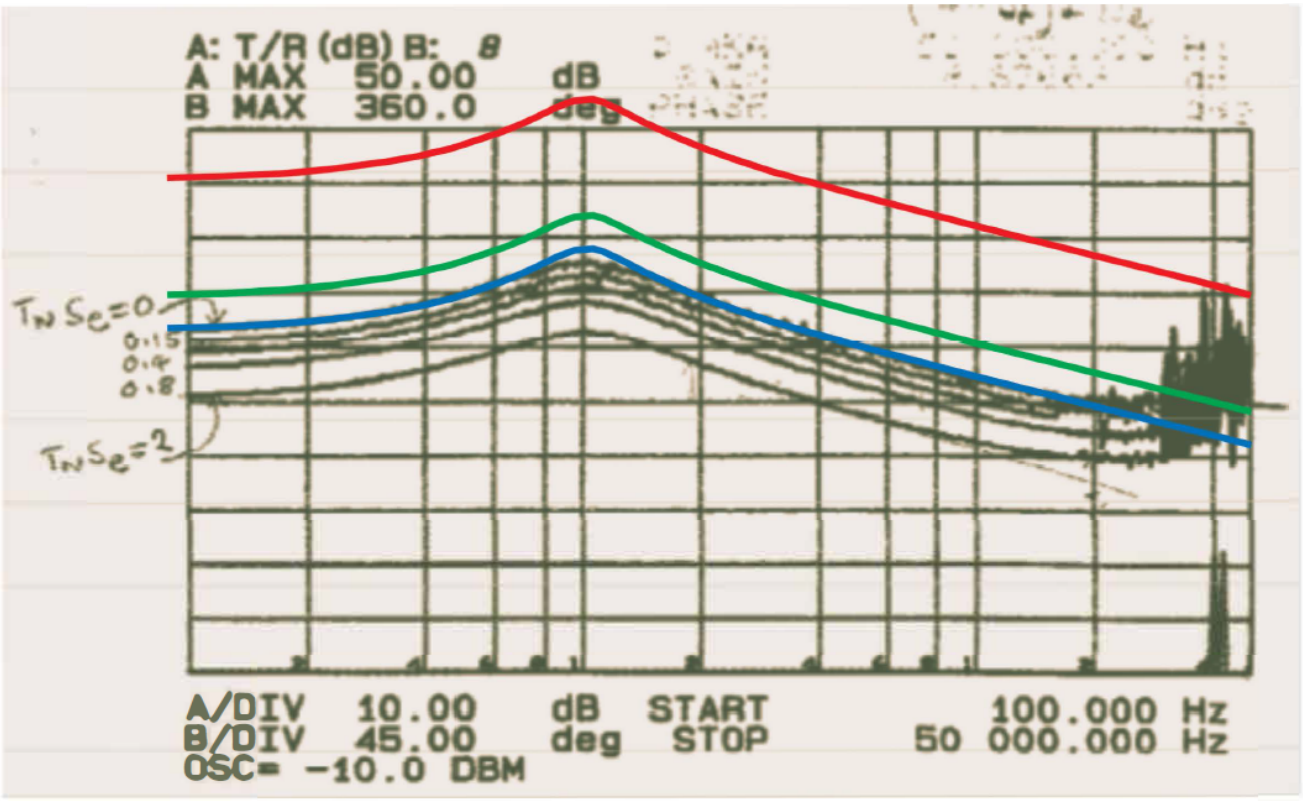


Figure A3.2: Original Lab Measurements Made in 1987 to Verify Modulator Gain

Measured current-loop gains made with a digital modulator. The black traces are for measurements with differing amounts of compensating ramp. The top black measurement is with no external ramp, and this agrees exactly with the predictions of Bello and Brown.

Modulator gains predicted by Middlebrook and Lee are shown to be wrong.

Note that Nyquist criterium is adhered to - none of the measured loop crossovers exceed half the switching frequency.

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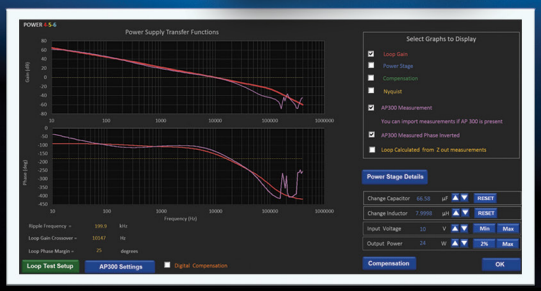
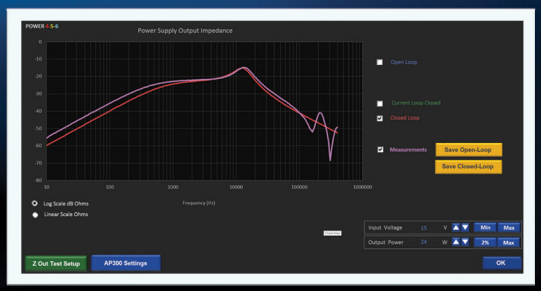
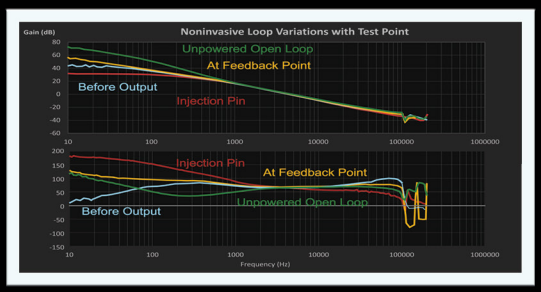
Power Supply Loop Gain

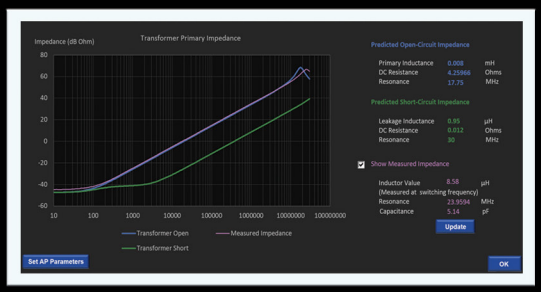


Power Supply Output Impedance





Noninvasive Loop Measurement



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4. Complete Small-Signal Model for Current-Mode Control

4.1 Introduction

In the previous chapter, an accurate continuous-time model was derived for the current-mode control cell with fixed input and output voltages. An invariant gain, $H_e(s)$, was derived for the feedback sampling gain for PWM converters with constant-frequency and variable-frequency control schemes. However, the form of the sampling gain is inconvenient for analytical investigation of the current-mode system since it contains exponential terms in s.

In this chapter, a second-order approximation is made to the sampling gain to provide a model which is accurate to half the switching frequency. The approxi-

mation is in simple polynomial form which will allow the subsequent derivation of analytical transfer functions which are useful for design purposes.

To complete the small-signal model around the current-mode cell, variations in input and output voltages must be allowed. The effects of changes in these quantities will be analyzed in this chapter, and modeled with simple feedforward terms into the duty cycle of the converter. The values of these feedforward terms will be derived for the general PWM switch model, and applied to the three basic two-state converters.

All of the modeling in Chapter 3 has been applied to converters in continuous-conduction mode. The final part of this chapter will cover the modeling of the PWM converters in discontinuous-conduction mode (DCM). It will be shown that no sampled-data modeling is required to derive the model of the DCM converters with current-mode control. All that is needed in the model is the standard DCM switch model, and feedforward terms from the input and output voltages.

4.2 Approximation to Sampling Gain Term

A common expression for all converters was found in Chapter 3 for the sampling gain, $H_e(s)$. This expression is not useful in itself for analytical insight into the

behavior of current-mode systems, and it must be approximated by a simpler function. Fig. 4.1 shows the plot of the exact transfer function, and Fig. 4.2 shows the location of the poles and zeros of the transfer function. The multiple poles of the function are derived from the condition

$$H_e(s_p) = \frac{s_p T_s}{e^{s_p T_s} - 1} = \infty \tag{4.1}$$

The finite solution of this condition is

$$e^{s_p T_s} = 1 \tag{4.2}$$

which is satisfied at frequencies which are integer multiples of the switching frequency. An obvious approach to approximating the transfer function of Eq. (4.1) is to use a continuous-time transfer function with the same poles and zeros in polynomial form. An approximation could then be made at lower frequencies by simply retaining only the lower-frequency poles of the polynomial transfer function. This is not a satisfactory approach. The exponential poles of Eq. (4.1) have infinite Q. However, even at frequencies well before the pole frequency, the phase of the transfer function is significantly altered, as can be seen in Fig. 4.1. Complex polynomial poles with infinite Q exhibit quite different behavior. The phase of a pair of infinite-Q polynomial poles is flat until the resonant frequency, at which point it drops down abruptly by 180 degrees. It does not make sense, therefore, to simply replace the exact expression for $H_e(s)$ with a polynomial expression with coincident poles and zero. Even though both transfer functions

would have the same peaking frequencies, the modeling of the phase characteristic would be very poor.

The objective of a simple model for the sampling gain is to match the gain and phase characteristics of the transfer function as closely as possible over the frequency range of interest. For the sampled-data system, the maximum frequency to be modeled is the Nyquist frequency, equal to half the switching frequency. Notice that the sampling gain function shown in Fig. 4.1 has a well-behaved characteristic up to half the switching frequency, with no discontinuities.

Many different approaches can be taken to match one complex transfer function to another over a prescribed frequency range. However, the sought-after model in the case of current-mode control has some special requirements. At dc, the transfer functions should match exactly, or the resulting new current-mode model would be less accurate at low frequencies than existing averaged models. Secondly, it is known that the oscillation problem inherent in current-mode control occurs at one-half the switching frequency, so the approximation to the transfer function should also be exact here.

A first-pass approximation to the sampling gain is a second-order polynomial. $H_e(s)$ exhibits a change in phase from zero to minus ninety degrees at half the switching frequency, and an increase in gain, as seen in Fig. 4.1. A first-order polynomial is inadequate for modeling such behavior since its maximum possible

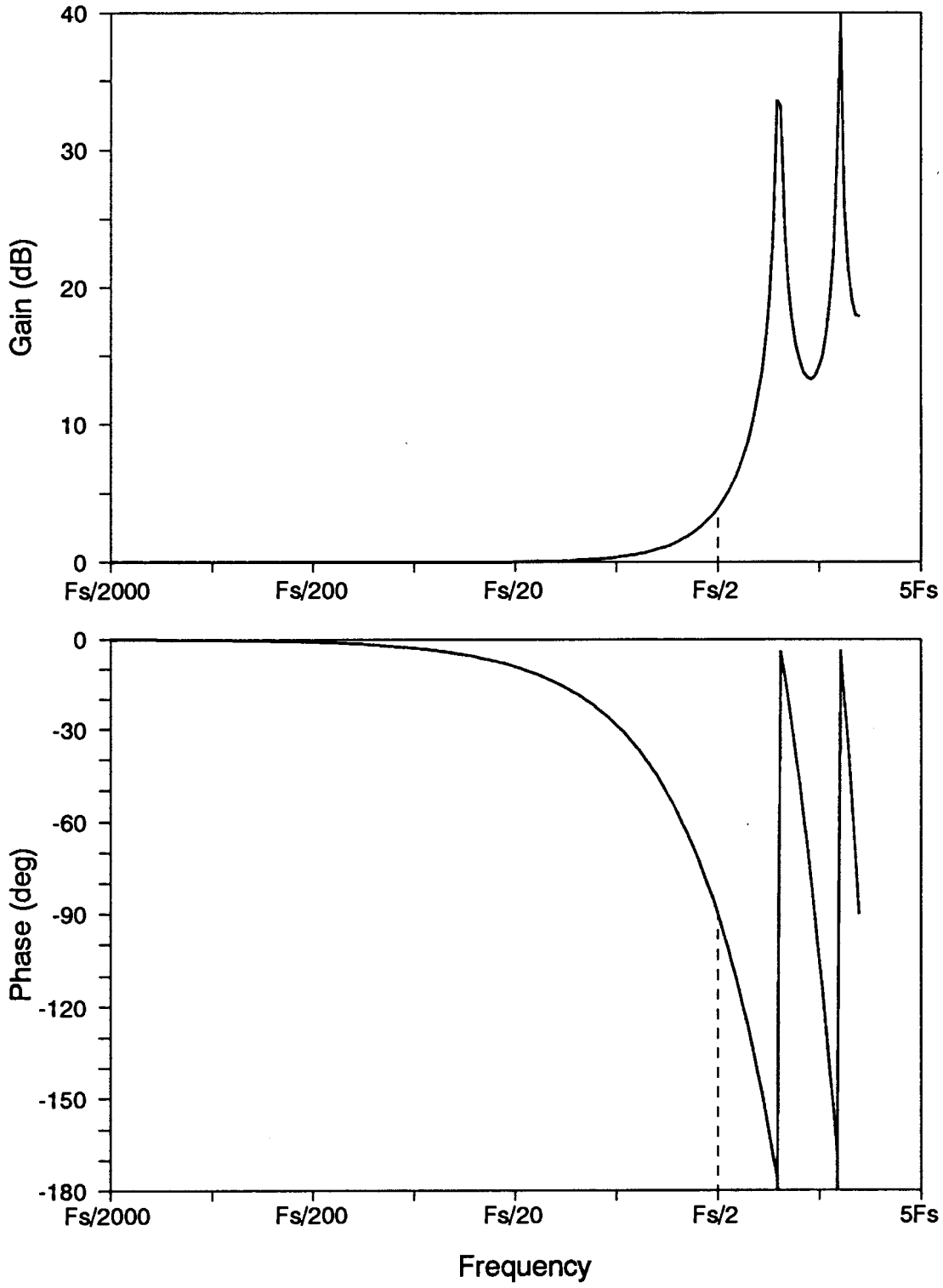


Figure 4.1. Exact Transfer Function for Sampling Gain: *At half the switching frequency the gain has increased by about 4 dB, and the phase shows exactly 90° lag. High-Q poles are apparent at the switching frequency and twice the switching frequency.*

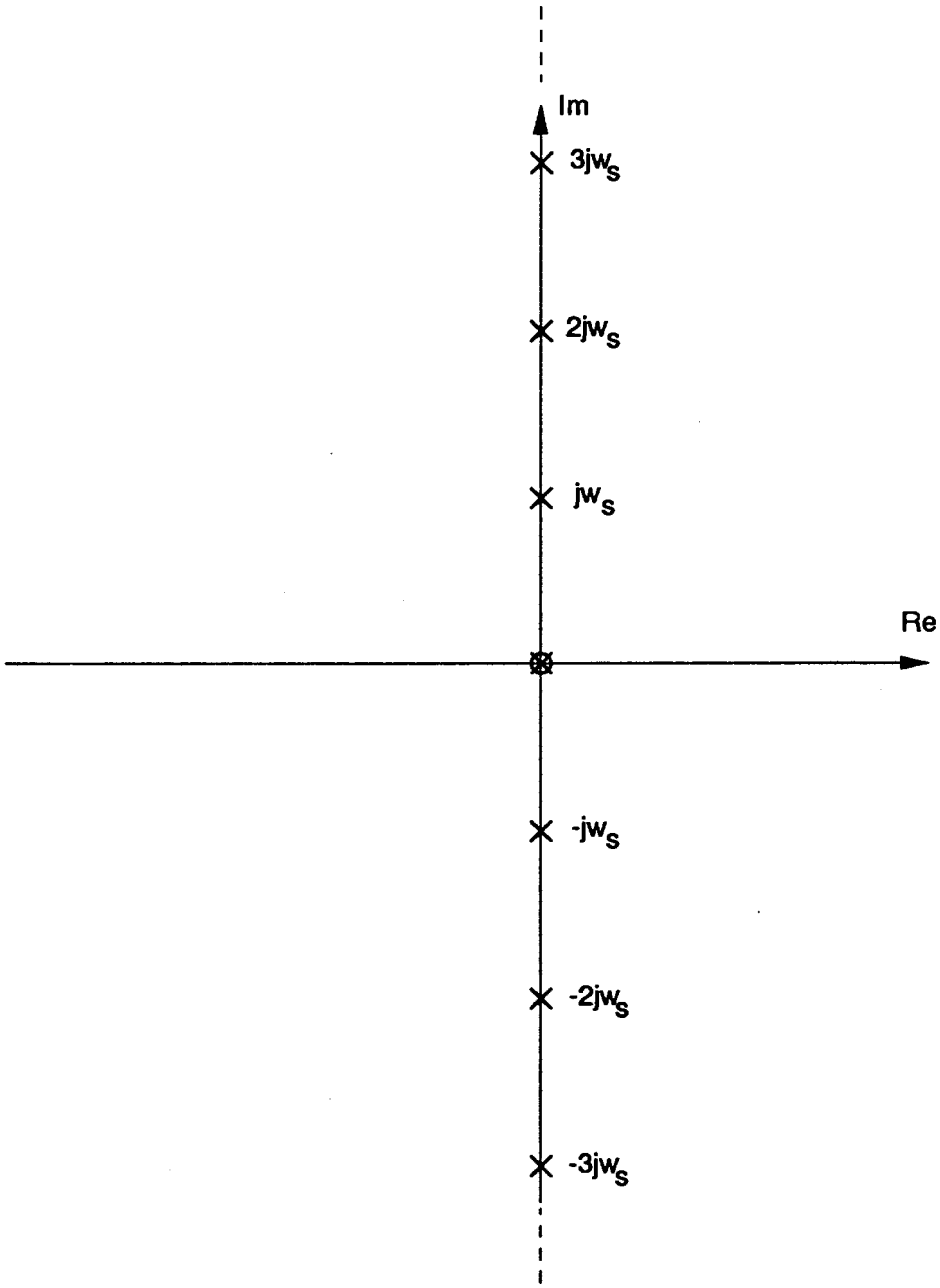


Figure 4.2. ***Pole-Zero Locations of the Exact Sampling Gain:*** *The exact sampling gain transfer function has a pole and a zero at the origin, and an infinite number of complex pole pairs occurring at each integer multiple of the switching frequency.*

phase delay is ninety degrees, obtainable only if the pole or zero is placed at the origin. An approximate expression is chosen such that

$$H_e(s) \simeq 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \tag{4.3}$$

This approximate expression is equal to unity at dc (s = 0), matching the value of the exact transfer function. At half the switching frequency, the approximate expression can be forced to equal the exact transfer function gain and phase exactly if parameters are chosen such that

$$Q_z = \frac{-2}{\pi} \tag{4.4}$$

and

$$\omega_n = \frac{\pi}{T_s} \tag{4.5}$$

This choice of parameters satisfies the end conditions exactly for the approximation, and will suffice if the deviations between the average and exact models are small at all frequencies in between. Fig. 4.3 shows the exact and approximate transfer functions plotted up to half the switching frequency. It can be seen from this figure that the approximate second-order model is very accurate. The gain does not deviate from the exact expression by more than 0.2 dB, and the phase by not more than 3 degrees.

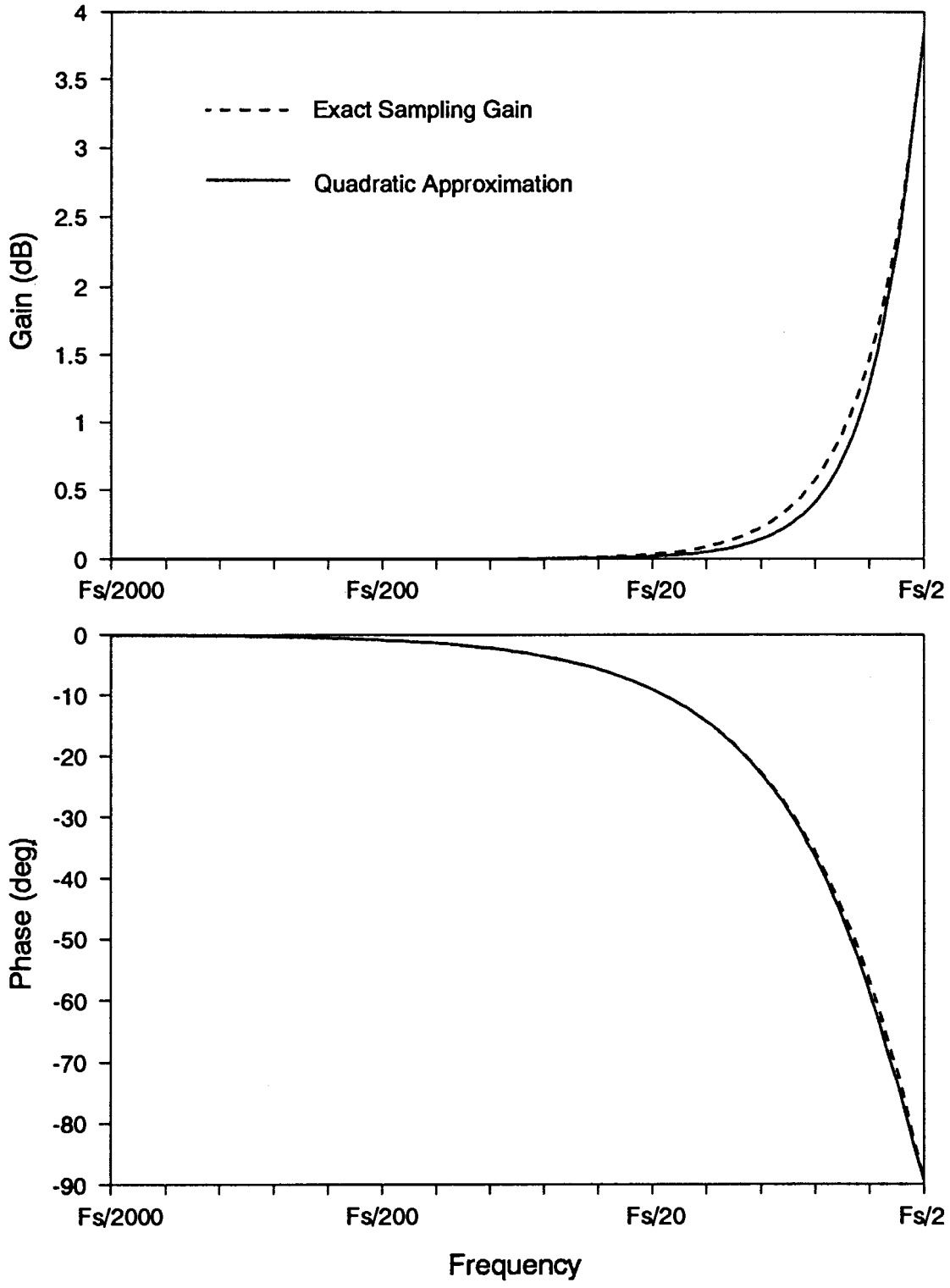


Figure 4.3. ***Exact Sampling Gain and Approximation:*** *The approximate sampling gain expression, given by a quadratic formula, is equal to the exact expression at dc and half the switching frequency, and differs by less than 0.2 dB and 3 degrees at all frequencies in between.*

4.3 Derivation of Feedforward Gains for CCM

The sampled-data model and the low-frequency approximation derived so far have been for the simple current-mode cell with fixed input and output voltages. Perturbations in these voltages must be allowed for to complete the new current-mode model. In current-mode control, it is the peak (or valley) of the current that is directly controlled by the modulator input voltage. It was shown in the previous chapter that perturbations away from steady-state of this controlled current peak lead to perturbations which were held constant over the whole switching cycle. It was not important that the peak current was the controlled quantity.

When deriving the complete current-mode model, however, the fact that the average current is different from the peak current is significant. In Fig. 4.4 the modulator waveforms are shown, and it can be seen that the average current in steady-state is equal to the peak current minus or plus half of the ripple current, depending on the control scheme being used. Furthermore, the ripple current is a function of the duty cycle, input voltage and output voltage of the current cell. As the input and output voltages are changed, there is a direct effect on the duty cycle and the average current value.

The effect of the input and output voltage perturbations can be modeled with the block diagram shown in Fig. 4.5. In addition to the model parameters derived in Chapter 3, feedforward gain terms from the input and output voltages to the duty

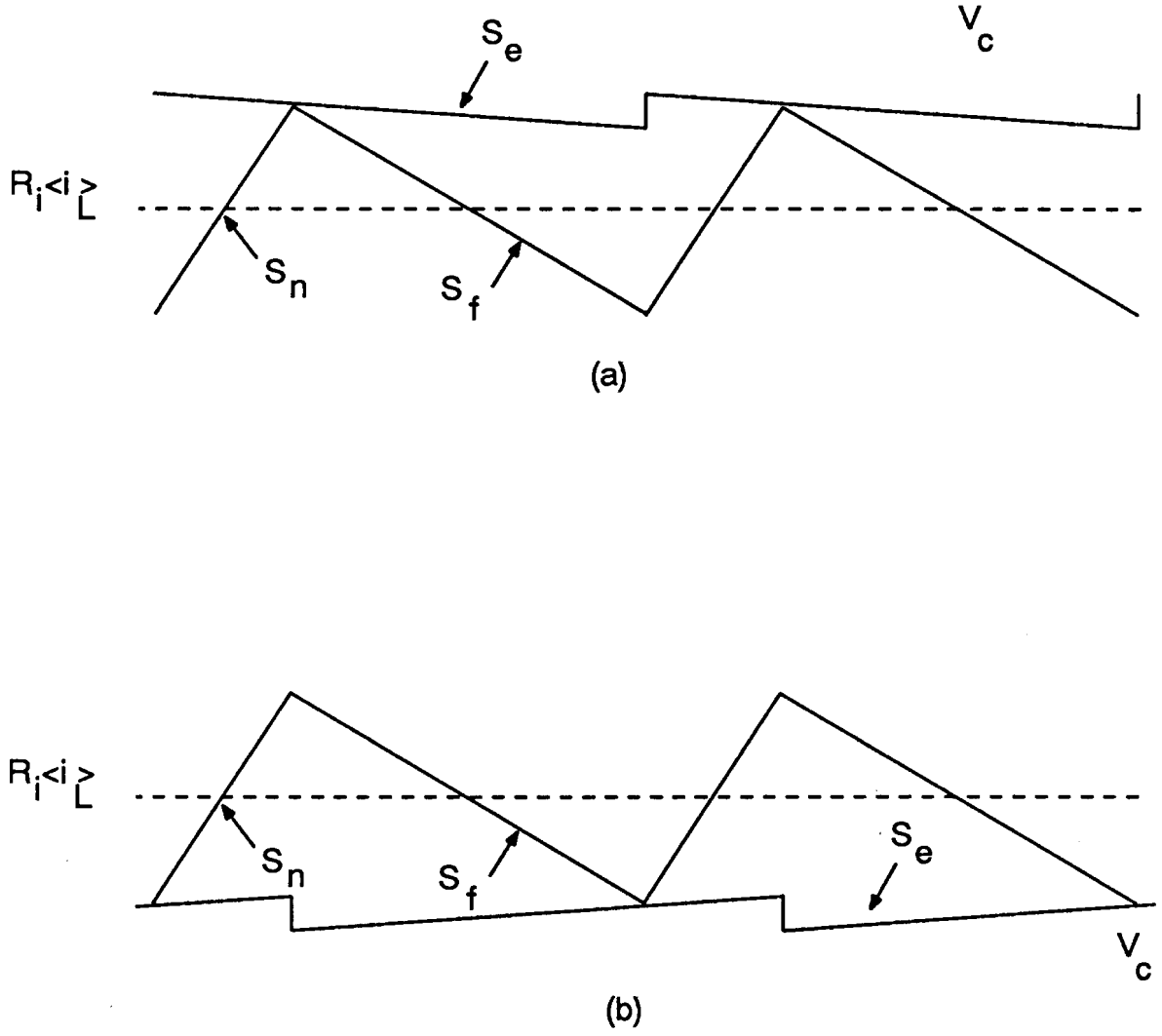


*Figure 4.4. **Steady-State Modulator Waveforms:** The average inductor current, $\langle i_L \rangle$ is related to the peak current and the ripple current. The ripple current is determined by the voltages across the inductor during the on and off times, and by the duty cycle.*

cycle are included. Notice that the modulator gain is included in the feedforward paths. This is an arbitrary choice which has the benefit of simplifying the expressions for the feedforward terms, and which will provide terms which are independent of the modulator gain parameters. A direct feedforward path from input or output voltage to duty cycle could be chosen, but this produces a more complex gain term which is dependent upon the modulator gain.

The model of Fig. 4.5 is useful for analytical derivation of the system transfer functions, and it is used for this purpose in the next chapter of this dissertation. However, it has the drawback that the gain terms, k_f and k_r, must be derived for each converter to be modeled. An alternative form of the current-mode model is shown in Fig. 4.6. In this representation, the feedforward terms are from the on-time voltage across the inductor, via k_f', and from the off-time voltage across the inductor, via k_r'. This model provides invariant values for these gains which is far more convenient when building the new current-mode model into a circuit analysis program such as Spice.

The models of Figs. 4.5 and 4.6 are, of course, intimately related. The on-time and off-time inductor voltages are linear combinations of the input and output voltages, and the model gains are also linear combinations of each other. By finding the values of k_f' and k_r' of Fig. 4.6, the gains k_f and k_r of Fig. 4.5 can be found with simple algebra. This saves a considerable amount of work in the derivations for each converter. The technique is applied in the analysis of this chapter.

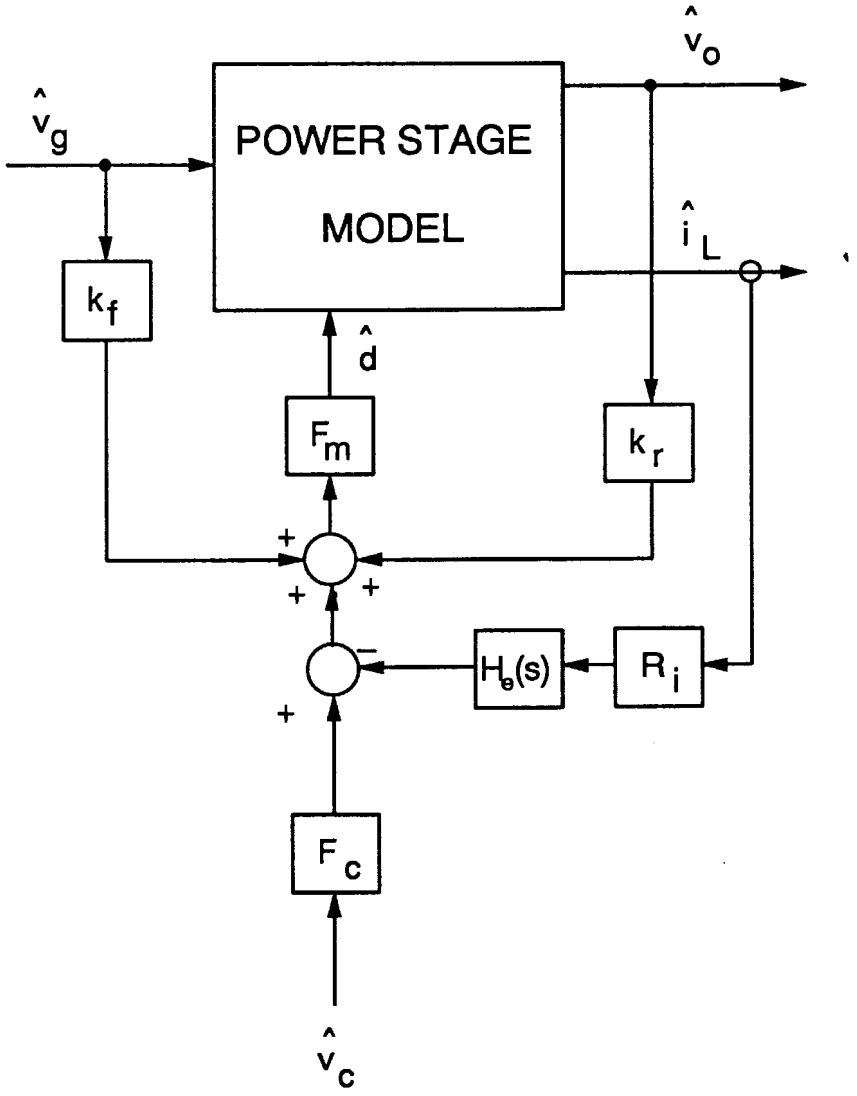


Figure 4.5. ***Complete Small-Signal Model for Current-Mode Control:*** *Feedforward terms from the input and output voltages complete the small-signal model to predict the effect on inductor current of changes in the input and output voltage. This form of the model is useful for transfer-function analysis, and is used in Chapter 5.*

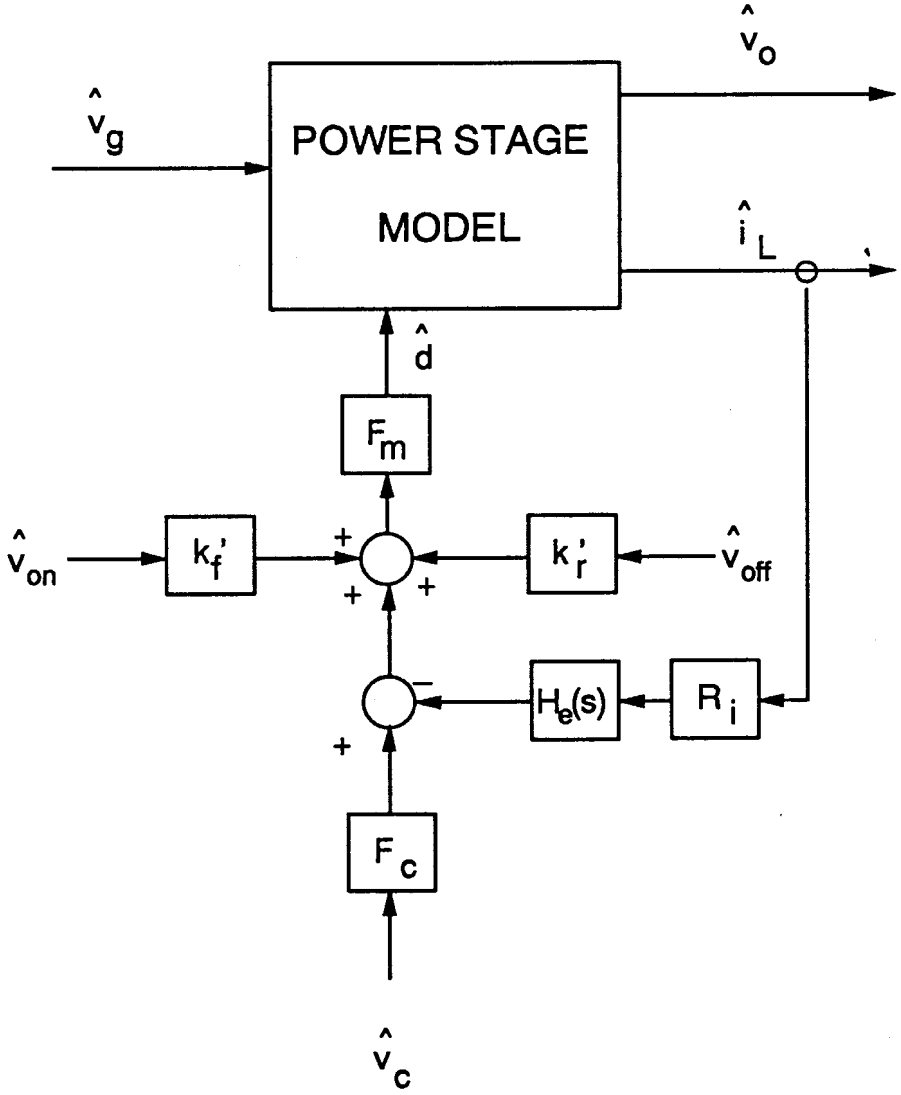


Figure 4.6. ***Invariant Small-Signal Model for Current-Mode Control:*** *Feedforward terms in this model are from the on-time and off-time voltages of the current cell. This form of the model has the advantage of invariance. The values of k_f' and k_r' are constant, regardless of the power stage topology. This is more useful for circuit analysis programs.*

The values of the feedforward terms, k_f' and k_r', can be found from the steady-state equation relating the average inductor current to the peak inductor current. Differentiation of this equation with respect to on-time and off-time voltages (one at a time) gives the small-signal perturbation of average inductor current. The block diagram of Fig. 4.6 can then be analyzed under steady-state conditions, and the value of the feedforward terms chosen to match the correct result.

Referring to the steady-state waveforms of Fig. 4.4, the describing function for the inductor current in terms of the control voltage and operating conditions, for constant frequency control with trailing-edge modulation, or for constant off-time control, is given by

$$R_i < i_L > = v_c - dT_s S_e - \frac{s_f d' T_s}{2} \qquad (4.6a)$$

For constant-frequency, leading-edge modulation and constant on-time control, the describing function is given by

$$R_i < i_L > = v_c + d' T_s S_e + \frac{s_f d' T_s}{2} \qquad (4.6b)$$

The quantity $< i_L >$ denotes the average value of inductor current under steady-state conditions.

The complete small-signal model for the current-mode cell is shown in Fig. 4.7. This model is obtained by inserting the generic current cell of Fig. 3.3 into the

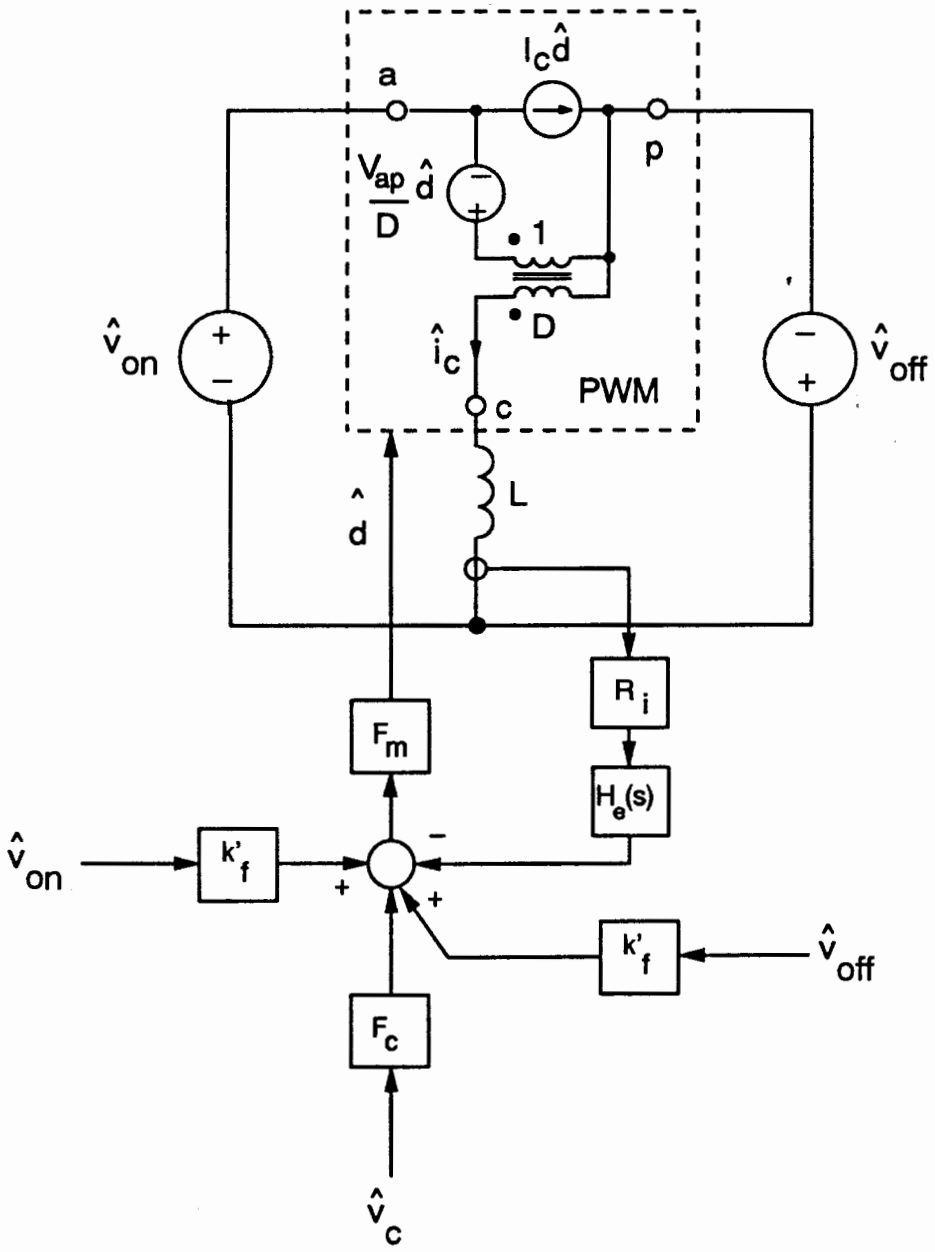


Figure 4.7. ***Small-Signal Model for the Generic Current Cell:*** *The input and output voltages of the generic cell are v_{on} and v_{off}, respectively. For the flyback converter, these are equal to the input and output voltages, and in general are linear combinations of the input and output voltages.*

block diagram of Fig. 4.6. For the generic current-mode cell shown in Fig. 4.7, the following equalities hold:

$$d = \frac{v_{off}}{v_{on} + v_{off}} \tag{4.7}$$

$$d' = \frac{v_{on}}{v_{on} + v_{off}} \tag{4.8}$$

and

$$s_f = \frac{v_{off} R_i}{L} \tag{4.9}$$

Substituting these expressions into the describing function of Eq. (4.6a) for the steady-state average current, and perturbing the on-time voltage, v_{on}, the small-signal perturbation in the average inductor current with respect to the on-time voltage is found for constant-frequency, trailing-edge modulation control:

$$\frac{\hat{<i_L>}}{\hat{v}_{on}} = \frac{DS_eT_s}{V_{ap}R_i} - \frac{D^2T_s}{2L} \tag{4.10}$$

The circuit diagram of Fig. 4.8 can be used to derive the same quantity, this time in terms of the feedforward gain, k_f'. The sampling gain term does not appear in Fig. 4.8 since it is unity at dc. The analysis is trivial when one recognizes that the inductor is a short circuit at dc, and the voltage across the inductor is zero

under steady-state conditions. For all forms of current-mode control, the gain is found to be:

$$\frac{\hat{<i_L>}}{\hat{v}_{on}} = \frac{1}{R_i}\left[\frac{D}{F_m V_{ap}} + k_f'\right] \tag{4.11}$$

The two expressions of Eqs. (4.10) and (4.11) can be equated to find the value of the feedforward gain. The value of F_m is dependent upon the form of current-mode control being used, and these values are summarized in Chapter 3. For constant-frequency, trailing-edge control,

$$F_m = \frac{1}{(S_n + S_e)T_s} \tag{4.12}$$

and the feedforward gain is found to be

$$k_f' = \frac{-DT_s R_i}{L}\left[1 - \frac{D}{2}\right] \tag{4.13}$$

A similar procedure is followed for the derivation of the feedforward gain from the off-time voltage. In this case, the describing function for the steady-state average current is perturbed with respect to the off-time voltage, v_{off}, and the small-signal perturbation in the average inductor current with respect to the off-time voltage is found for constant-frequency control to be:

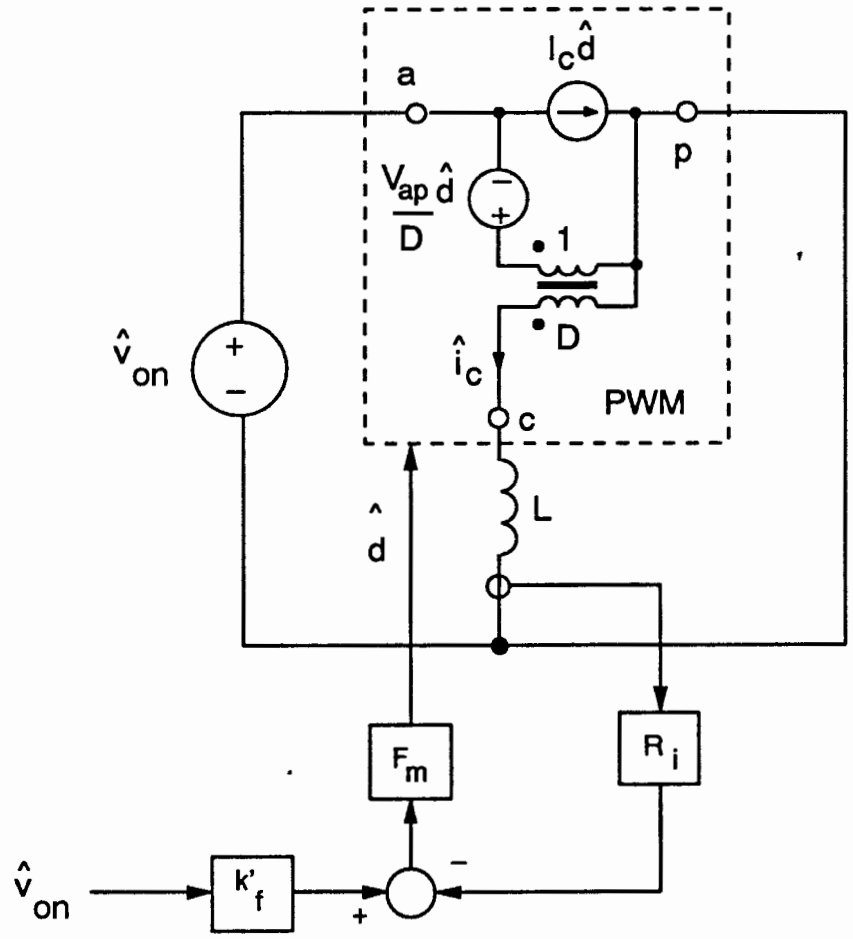


Figure 4.8. ***Generic Current Cell with Fixed Voltage During Off-Time:*** *The on-time voltage, which is in general a linear combination of input and output voltages, is allowed to vary, and the value of feedforward term, k_f', is derived for all converters.*

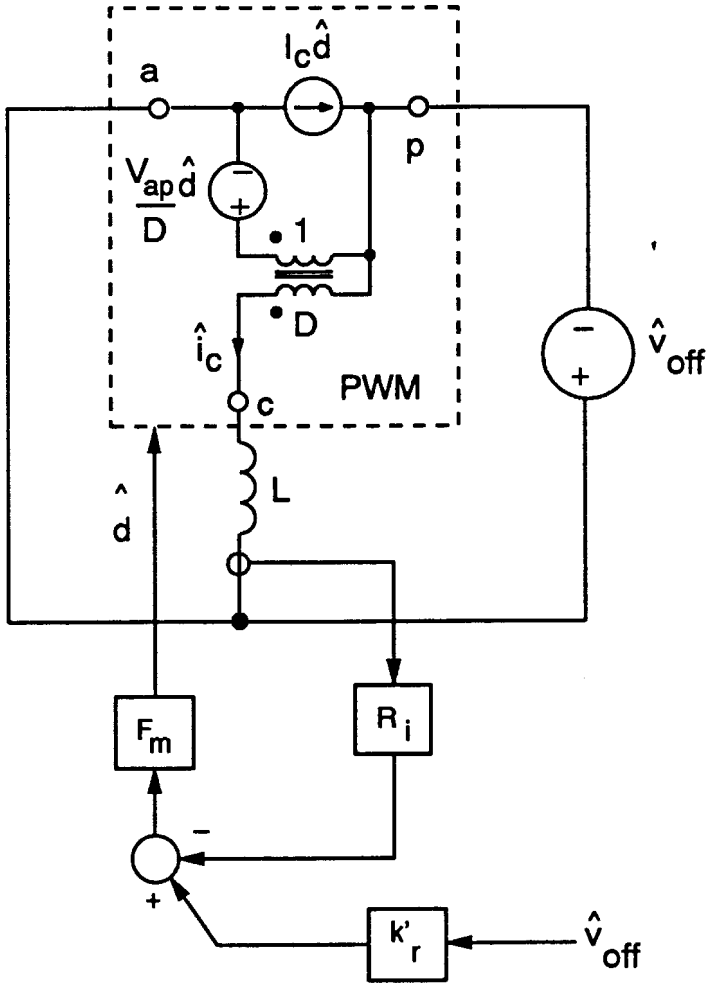


Figure 4.9. ***Generic Current Cell with Fixed Voltage During On-Time:*** *The off-time voltage, again a linear combination of input and output voltages, is allowed to vary in this case, and the value of feedforward term, k_r', is derived for all converters.*

$$\frac{\langle \hat{i}_L \rangle}{\hat{v}_{off}} = \frac{-D' S_e T_s}{V_{ap} R_i} - \frac{D'^2 T_s}{2L} \tag{4.14}$$

The circuit diagram of Fig. 4.9 can also be used to derive the same quantity, this time in terms of the feedforward gain, k_r'. The voltage across the inductor is again zero under steady-state conditions. Using this fact, the gain is found for all forms of current-mode control to be:

$$\frac{\langle \hat{i}_L \rangle}{\hat{v}_{off}} = \frac{1}{R_i} \left[\frac{-D'}{F_m V_{ap}} - k_r' \right] \tag{4.15}$$

The two expressions (4.14) and (4.15) can be equated to find the value of the feedforward gain from the off-time voltage for constant-frequency control:

$$k_r' = \frac{D'^2 T_s R_i}{2L} \tag{4.16}$$

This procedure can be repeated for constant on-time and constant off-time control, and the results for the feedforward gains of the generic current-mode cell are presented in Table 4.1.

Derivation of these gains completes the model of Fig. 4.6, and this model is used in Appendix B of this dissertation to generate equivalent circuit models in PSpice. The gains of the model are also used to derive the feedforward terms of Fig. 4.5 from the input and output voltages. As mentioned before, the on-time and off-

time voltages of the current-mode cell are linear combinations of the input and output voltages. The relationships between these voltages are summarized in Table 4.2 for the three basic PWM converters.

From this table, it can be seen that the on-time voltage for the buck converter is given by $V_g - V_o$, and the off-time voltage is given by V_o. A feedforward path from the input voltage is provided by the feedforward gain k_f' only. Feedforward of the output voltage is provided by both k_f' and k_r'. The specific feedforward gains for the buck converter are therefore calculated from

$$k_f = k_f' = \frac{-DT_sR_i}{L}\left[1 - \frac{D}{2}\right] \tag{4.17}$$

The feedforward gain from the output voltage is found to be:

$$k_r = k_r' - k_f' = \frac{T_sR_i}{2L} \tag{4.18}$$

This process can easily be followed for any PWM converter. The subsequent results for the buck, boost, and flyback converters are summarized in Table 4.3-4.6, where the feedforward gains with different control schemes are given. The derivation of these gains completes the new small-signal model for current-mode control in continuous-conduction mode.

TABLE 4.1
Feedforward Gains for Invariant Current-Mode Model

	Constant Frequency Trailing Edge	Constant Frequency Leading Edge	Constant Off-Time	Constant On-Time
k_f'	$-\frac{DT_s R_i}{L}\left[1-\frac{D}{2}\right]$	$-\frac{D^2 T_s R_i}{2L}$	$-\frac{DT_s R_i}{L}$	$-\frac{DT_s R_i}{2L}$
k_r'	$\frac{D'^2 T_s R_i}{2L}$	$\frac{D'T_s R_i}{L}\left[1-\frac{D'}{2}\right]$	$\frac{D'T_s R_i}{2L}$	$\frac{D'T_s R_i}{L}$

TABLE 4.2
Input and Output Voltage Relationships

	Buck	Boost	Buck-Boost
V_{on}	$V_g - V_o$	V_g	V_g
V_{off}	V_o	$V_o - V_g$	V_o
k_f	k_f'	$k_f' - k_r'$	k_f'
k_r	$-k_f' + k_r'$	k_r'	k_r'

TABLE 4.3
Feedforward Gains for Constant-Frequency, Trailing-Edge Control

	Buck	Boost	Buck-Boost
k_f	$-\frac{DT_s R_i}{L}\left[1-\frac{D}{2}\right]$	$-\frac{T_s R_i}{2L}$	$-\frac{DT_s R_i}{L}\left[1-\frac{D}{2}\right]$
k_r	$\frac{T_s R_i}{2L}$	$\frac{D'^2 T_s R_i}{2L}$	$\frac{D'^2 T_s R_i}{2L}$

TABLE 4.4
Feedforward Gains for Constant-Frequency, Leading-Edge Control

	Buck	Boost	Buck-Boost
k_f	$-\frac{D^2 T_s R_i}{2L}$	$\frac{T_s R_i}{2L}$	$-\frac{D^2 T_s R_i}{2L}$
k_r	$-\frac{T_s R_i}{2L}$	$\frac{D' T_s R_i}{L}\left[1-\frac{D'}{2}\right]$	$\frac{D' T_s R_i}{L}\left[1-\frac{D'}{2}\right]$

TABLE 4.5
Feedforward Gains for Constant Off-Time Control

	Buck	Boost	Buck-Boost
k_f	$-\frac{DT_s R_i}{L}$	$-(1+D)\frac{T_s R_i}{2L}$	$-\frac{DT_s R_i}{L}$
k_r	$(1+D)\frac{T_s R_i}{2L}$	$\frac{D' T_s R_i}{2L}$	$\frac{D' T_s R_i}{2L}$

TABLE 4.6
Feedforward Gains for Constant On-Time Control

	Buck	Boost	Buck-Boost
k_f	$-\frac{DT_s R_i}{2L}$	$-(1+D')\frac{T_s R_i}{2L}$	$-\frac{DT_s R_i}{2L}$
k_r	$(1+D')\frac{T_s R_i}{2L}$	$\frac{D'T_s R_i}{L}$	$\frac{D'T_s R_i}{L}$

4.4 Current-Mode Models for DCM

When operating in the discontinuous mode, the PWM switch model for DCM, shown in Fig. 4.10, must be used. The power stage models are obtained by substituting this model in the circuits of Fig. 4.1. The CCM converters needed sampled-data analysis to develop the small-signal models for current-mode control. This is not the case for converters operating in the DCM region.

Fig. 4.11 shows the modulator waveforms for a converter operating with current-mode control in DCM. The control reference is used with the sensed inductor current to control the turn-off of the power switch. For DCM, the inductor current always starts at zero at turn-on. It is possible to achieve exactly the same effect as current-mode control by using a simple sawtooth ramp whose

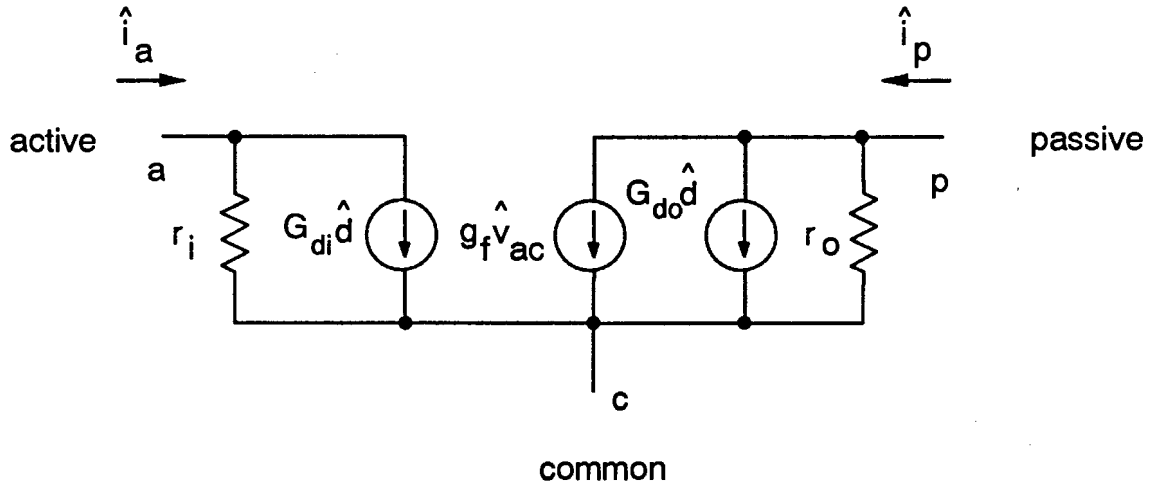


Figure 4.10. ***PWM Switch Model for Discontinuous-Conduction Mode.:*** *The PWM switch model for DCM is different from the model for CCM. It is invariant for all PWM converters.*

slope is determined by the input voltage, output voltage, and inductor value. Inductor current feedback is not necessary. The block diagram of Fig. 4.12 is, therefore, sufficient to completely model the current-mode feedback for DCM. The only task to be done to complete the model is to find the gains, k_f and k_r. As for the CCM model of Fig. 4.5, the model in Fig. 4.12 provides analytical insight, and is used for this purpose in Chapter 5. However, the model of Fig. 4.13 is more practical for circuit modeling since it has invariant gains for all converters. Notice that there is no gain term from the inductor off-time voltage in this model. It is shown below that the gain from this voltage is always zero.

The describing function of the modulator, expressing the on-time in terms of the control voltage and circuit conditions, for converters in DCM with a controlled on-time is given by

$$t_{on} = \frac{v_c}{s_n + S_e} \tag{4.19}$$

The on-time slope, s_n, is a function of on-time voltage, inductor value, and current-sense gain value, R_i. The small-signal perturbation due to changes in on-time voltage can therefore be found by taking the partial derivative of Eq. (4.19) with respect to this voltage. For the current-mode cell, the small-signal gains are given by

$$\frac{\hat{t}_{on}}{\hat{v}_{on}} = \frac{-DR_i}{L} \frac{1}{S_n + S_e} \tag{4.20}$$

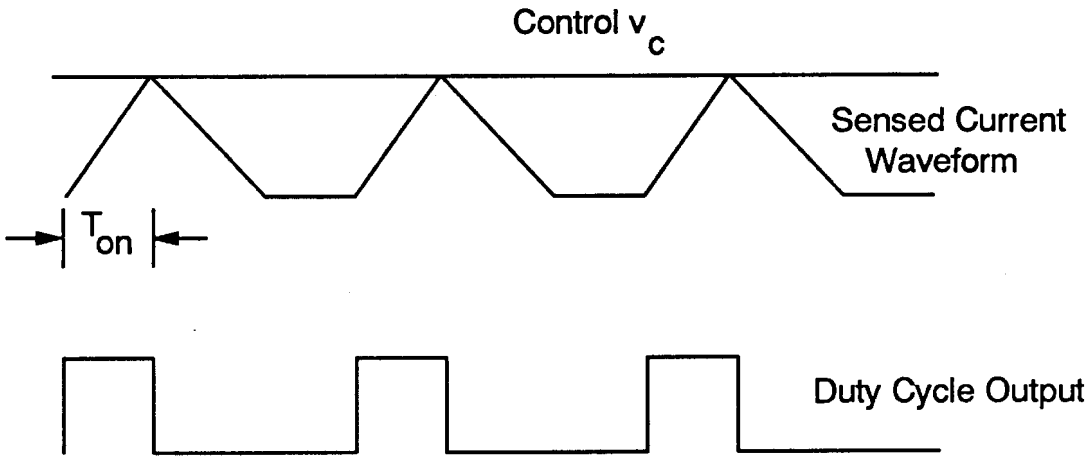


Figure 4.11. ***Discontinuous-Conduction Modulator Waveforms for Current-Mode Control.:*** *The sensed current waveform added to an external ramp is compared with a control signal, v_c, to provide the controlled duty cycle. Notice that the current ramp always starts from zero, and its slope is dependent upon the voltage across the inductor during the on-time.*

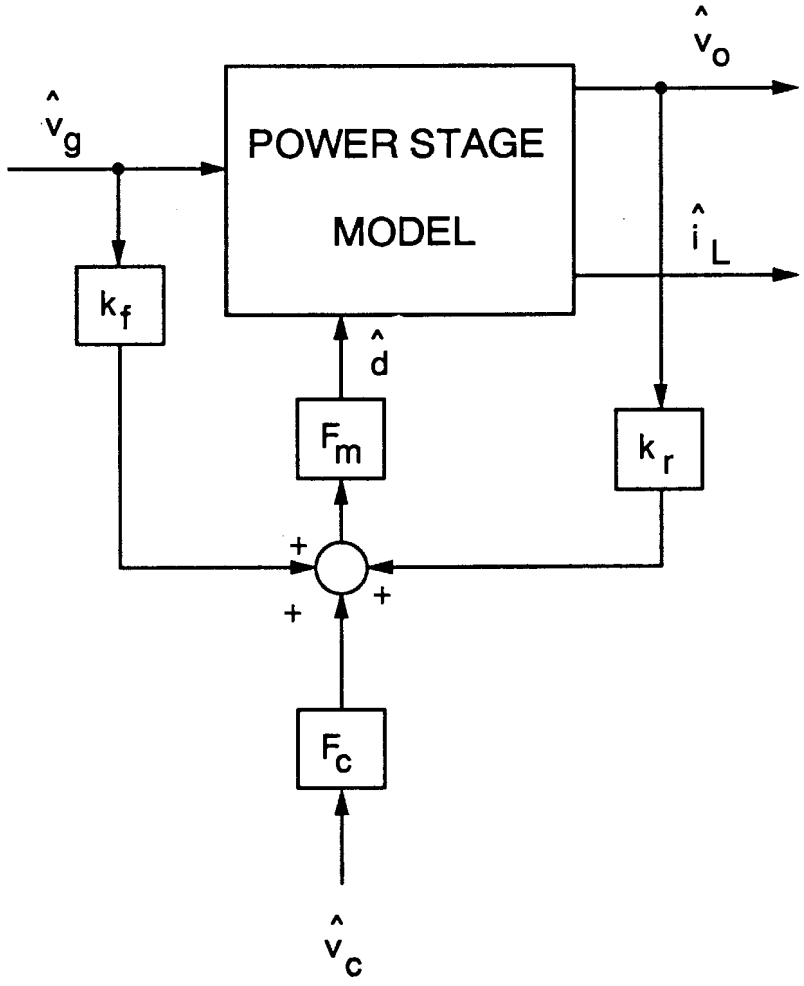


Figure 4.12. Small-Signal Block Diagram for Current-Mode Control (DCM): There is no feedback of inductor current in this block diagram, and no sampled-data modeling is needed. The feedforward blocks, k_f and k_r, provide the necessary control information.

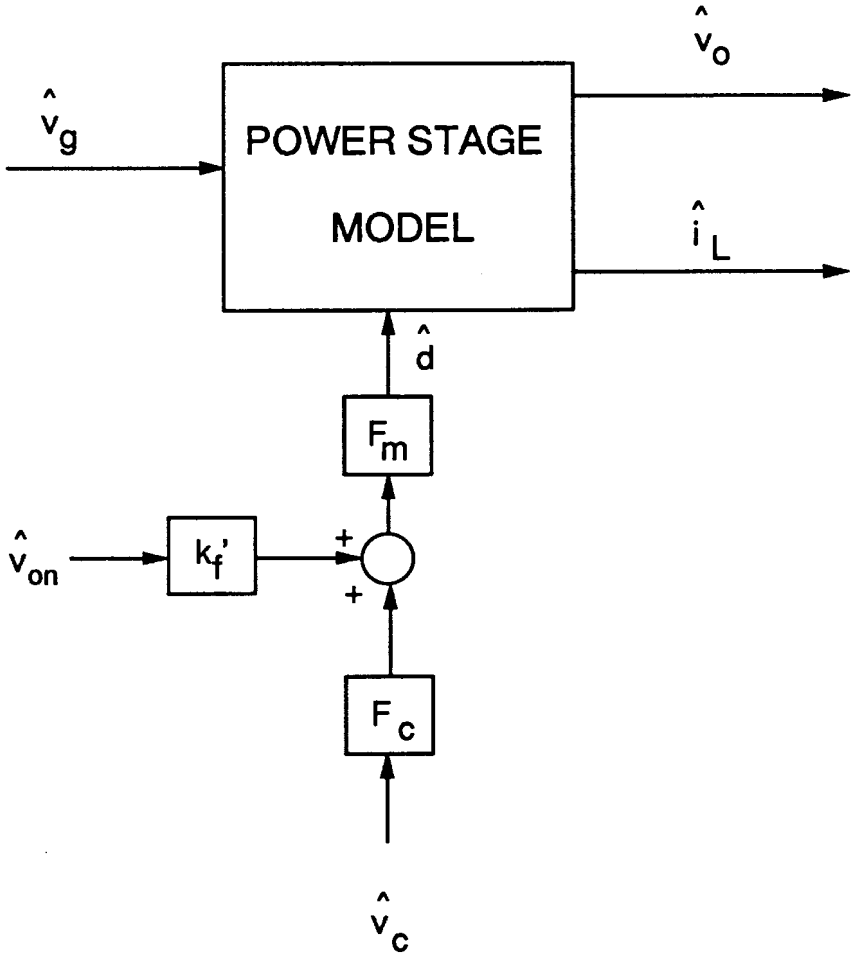


Figure 4.13. Invariant Model for Current-Mode Control (DCM): Only the feedforward gain, k_f', from the on-time voltage is needed in this form of the model. The value of this parameter is the same for all converters being modeled.

and, since the on-time does not depend upon the off-time slope,

$$\frac{\hat{t}_{on}}{\hat{v}_{off}} = 0 \tag{4.21}$$

For constant-frequency control, the perturbations in duty cycle are then given by

$$\frac{\hat{d}}{\hat{v}_{on}} = \frac{-DR_i}{L} \frac{1}{(S_n + S_e)T_s} \tag{4.22}$$

and

$$\frac{\hat{d}}{\hat{v}_{off}} = 0 \tag{4.23}$$

For constant off-time control, the gains with respect to the duty cycle are

$$\frac{\hat{d}}{\hat{v}_{on}} = -\frac{D'DR_i}{L} \frac{1}{S_n T_s} \tag{4.24}$$

and

$$\frac{\hat{d}}{\hat{v}_{off}} = 0 \tag{4.25}$$

Constant on-time current-mode control, and constant-frequency with leading-edge modulation cannot be implemented since there is no current signal available at the end of the off-time in DCM.

In the model of Fig. 4.13, perturbations in the duty cycle are given by the product of the gain k_f' and the modulator gain, F_m. This representation provides a more

convenient model. The necessary gains can be found by dividing Eqs. (4.22) and (4.24) by the modulator gain, resulting in the same expressions for both constant frequency and constant off-time control.

$$k_f' = -\frac{DT_sR_i}{L} \tag{4.26}$$

The gains for the generic current-mode cell can be translated into specific gains for each of the converters by using the relationships between the input and output voltages summarized in Table 4.2. The results of the analysis are presented in Table 4.7, for both constant-frequency and constant off-time control. Modulator gains for these control schemes, repeated here for convenience, are the same as those for continuous conduction mode.

TABLE 4.7

Summary of Gain Parameters for DCM

	Buck	Boost	Buck-Boost
k_f	$-\frac{DT_s R_i}{L}$	$-\frac{DT_s R_i}{L}$	$-\frac{DT_s R_i}{L}$
k_r	$\frac{DT_s R_i}{L}$	0	0
F_m	$\frac{1}{(S_n + S_e)T_s}$ (Constant Frequency) $\frac{D'}{S_n T_s}$ (Constant Off Time)		
F_c		1 (Constant Frequency) $e^{sDT_s/2}$ (Constant Off Time)	

4.5 Conclusions

The complex expression for the sampling gain, $H_e(s)$, derived in Chapter 3 was simplified with an approximate expression. A second-order polynomial was sufficient to accurately model the effects of the sampling action of current-mode control up to half the switching frequency. The approximate sampling gain is given by

$$H_e(s) \simeq 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \tag{4.27}$$

where

$$Q_z = \frac{-2}{\pi} \tag{4.28}$$

and

$$\omega_n = \frac{\pi}{T_s} \tag{4.29}$$

This simple transfer function gives remarkable accuracy in approximating the exact transfer function, both in gain and phase predictions. At dc and half the switching frequency, the functions are identical. It is not surprising that the second order transfer function is adequate, since the nature of the problem in the current-feedback system is an oscillation, normally associated with a pair of complex poles in the system. It will be seen in the next chapter how the complex zeros of the approximation to the sampling gain produce a corresponding pair of complex poles in the closed-loop system. An interesting feature of the sampling gain approximation is that it has complex zeros in the right-half plane. The im-

portance of this in modeling system performance will also be discussed in the next chapter.

The small-signal model for continuous-conduction mode was completed with the derivation of feedforward gains from the on-time and off-time voltages across the inductor. These gains were then used to derive the individual feedforward gains for specific converters from the input and output voltages. The invariant form of the model with feedforward from on-time and off-time voltages is very useful for circuit modeling. The model with feedforward from input and output voltages can provide more analytical insight into some of the observed phenomena of current-mode control. The impact of the feedforward gains on the small-signal performance will be discussed in the next chapter.

Finally, the small-signal model for current-mode control with discontinuous inductor current was derived. Simple arguments show that a current-feedback loop is not even needed in the small-signal model, and sampled-data analysis is not needed for the DCM model. Feedforward gain terms provide the complete model for the system when coupled with an accurate model for the power stage.

5. Predictions of the New Current-Mode Control Model

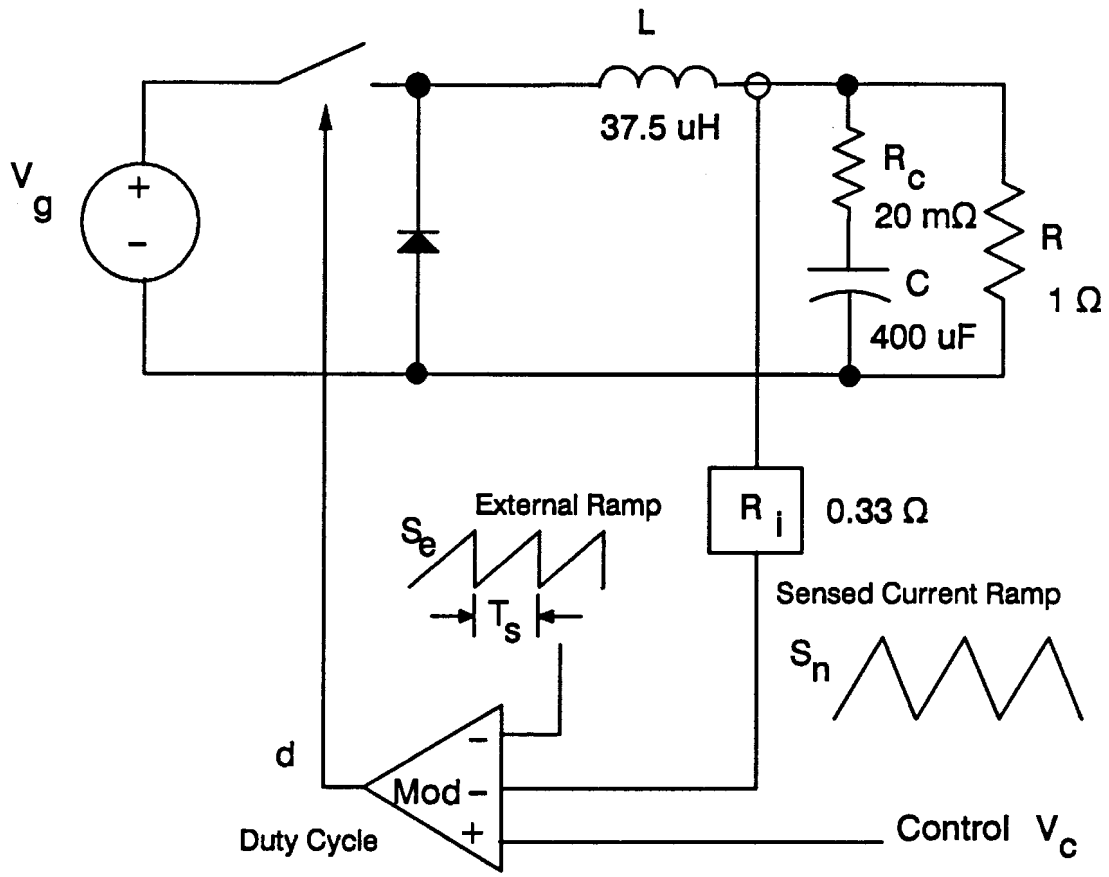
5.1 Introduction

In the previous two chapters, a new small-signal model for current-mode control was derived for converters operating in continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM), with several different forms of controllers. In this chapter, the new model will be applied to a power converter to derive some of the interesting transfer functions that result from current-mode control. This will demonstrate how the new current-mode model overcomes the shortcomings and difficulties of previous modeling approaches and provides design insight to the system. Transfer function predictions are confirmed with measurements on an experimental power stage.

5.2 Constant-Frequency Control in CCM

The buck converter shows some of the most interesting properties with current-mode control, and was therefore chosen as an example to demonstrate the features of the new current-mode model. Fig. 5.1 shows the converter used as an example throughout this chapter, with the component values. Ideal switches were assumed. The converter was operated in this section with constant-frequency control at 50 kHz, with the clock initiating the on-time. The inductor current waveform was scaled by a sensing network by 0.33, and the external ramp slope, S_e, was adjustable to show the effect of changing the ramp. The component values of this converter were combined with the current-mode model to provide the analytical predictions derived in this chapter. Transfer functions were plotted by modeling the circuit and current-mode model in PSpice, as described in Appendix B.

An experimental converter, shown in Fig. 5.2 was also built to make hardware measurements of the small-signal transfer functions. This circuit was used throughout this chapter. Fig 5.2 shows the essential features of the current-mode control circuit, using the UC3825 control chip from Unitrode [39]. Protection features, bypass capacitors, and supply voltages are not shown in the circuit diagram.



$T_s = 20$ us

$V_o = 5$ V

*Figure 5.1. **Example Buck Converter for Confirmation of Small-Signal Predictions:** The buck converter has some of the most interesting characteristics with current-mode control and was chosen to confirm the modeling approach.*

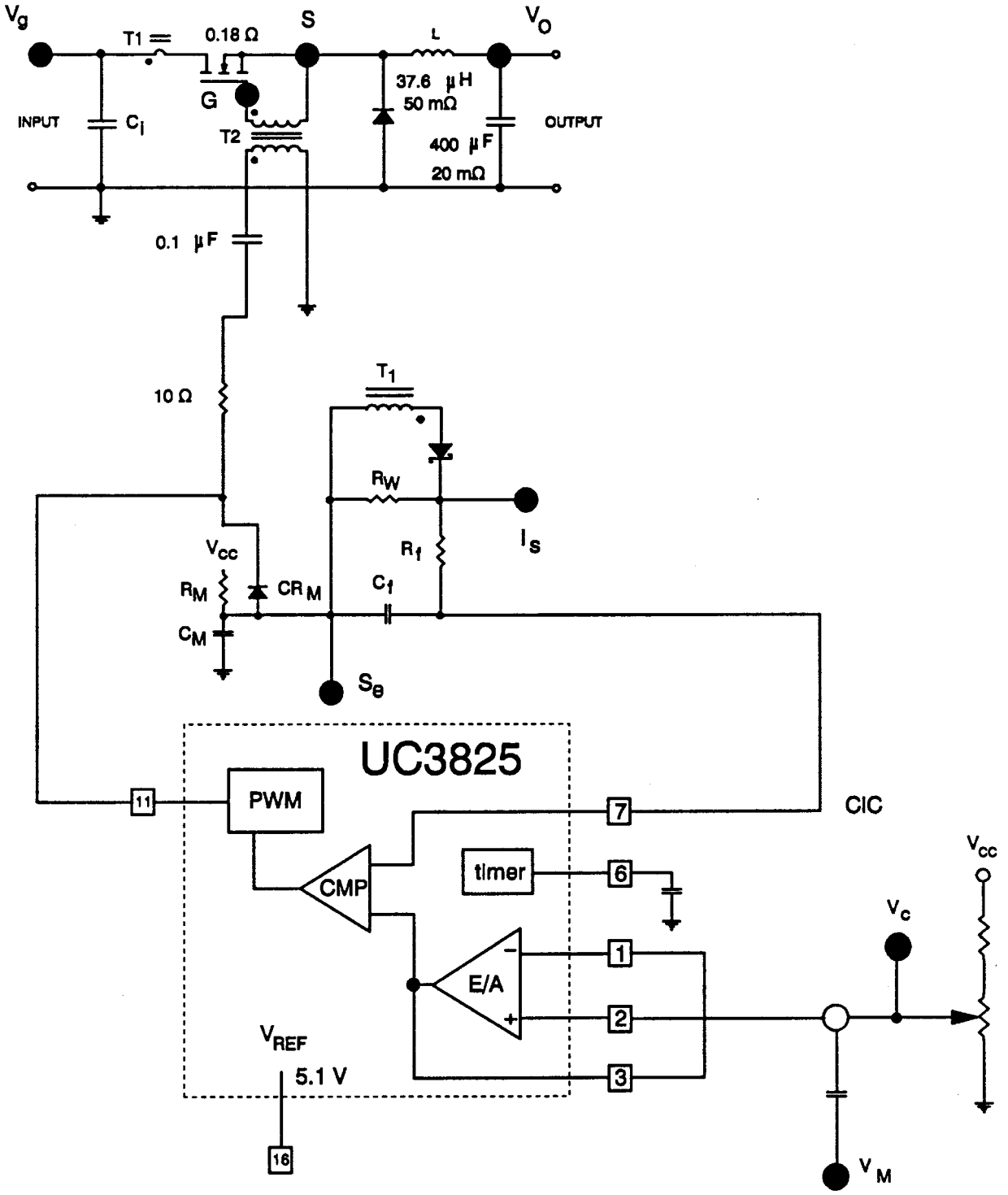


*Figure 5.2. **Experimental Buck Converter for Small-Signal Measurements:** An experimental circuit was built to confirm the predictions of the model with measured data. The essential components and functions of the current-mode control are shown in this circuit diagram.*

The effective current sensing gain, R_i, of Fig. 5.1, was actually implemented in the hardware circuit by a current transformer, T_1, in series with the power switch. The current transformer turns ratio, and the current sense resistor, R_w, set the gain of the sensing network to be 0.33. A high-frequency filter, formed by components R_f and C_f, was used to filter out switching spikes.

An external ramp was created by the components R_m, C_m and CR_m. The capacitor was charged up through R_m from the supply voltage of the control chip when the gate drive signal was high, and discharged through the diode, CR_m, when the gate drive signal was low. The small amplitude of the external ramp, typically less than 2 V, compared to the supply voltage of 16 V, ensured that the external ramp was linear. The amplitude of the external ramp was adjusted by selecting the appropriate value of resistor, R_m.

The operating point of the control and power stage circuit was set by adjusting the dc value of the control voltage, V_c, with a potentiometer. Modulations in the control voltage could be introduced via the connection V_m. The error amplifier of the circuit, connected to pins 1-3, was configured as a voltage follower, so the output of the amplifier was always equal to the control voltage, V_c.

5.2.1 Current Loop Gain

Current-mode control uses feedback of the inductor current to improve the characteristics of the power stage. As with any feedback system, it is instructive to look at the loop gain of the current feedback to ensure that the system is stable for all conditions. Usually, loop gain is also used for designing the compensation of the feedback system. However, current-mode control of the form analyzed in this thesis uses only gain in the current feedback network, and there is little design freedom.

Fig. 5.3 shows the new small-signal model for current-mode control, applied to the buck converter to derive the current loop gain, $T_i(s)$. The current loop is created by feedback of the current state through the sensing gain, R_i. A second feedback block, k_r, is created when the current loop is closed, but it is easy to show that this block is only significant when the converter operates close to DCM. Even then, the effect of this gain is only significant at low frequencies. The feedforward gain, k_f, from the input voltage is not shown since the input voltage perturbations are zero when deriving the current loop gain.

Ignoring the gain term k_r, the approximate expression for the current loop gain, $T_i(s)$, is given by:

$$T_i(s) \simeq \frac{L}{RT_s m_c D'} \frac{1 + sCR}{\Delta(s)} H_e(s) \tag{5.1}$$

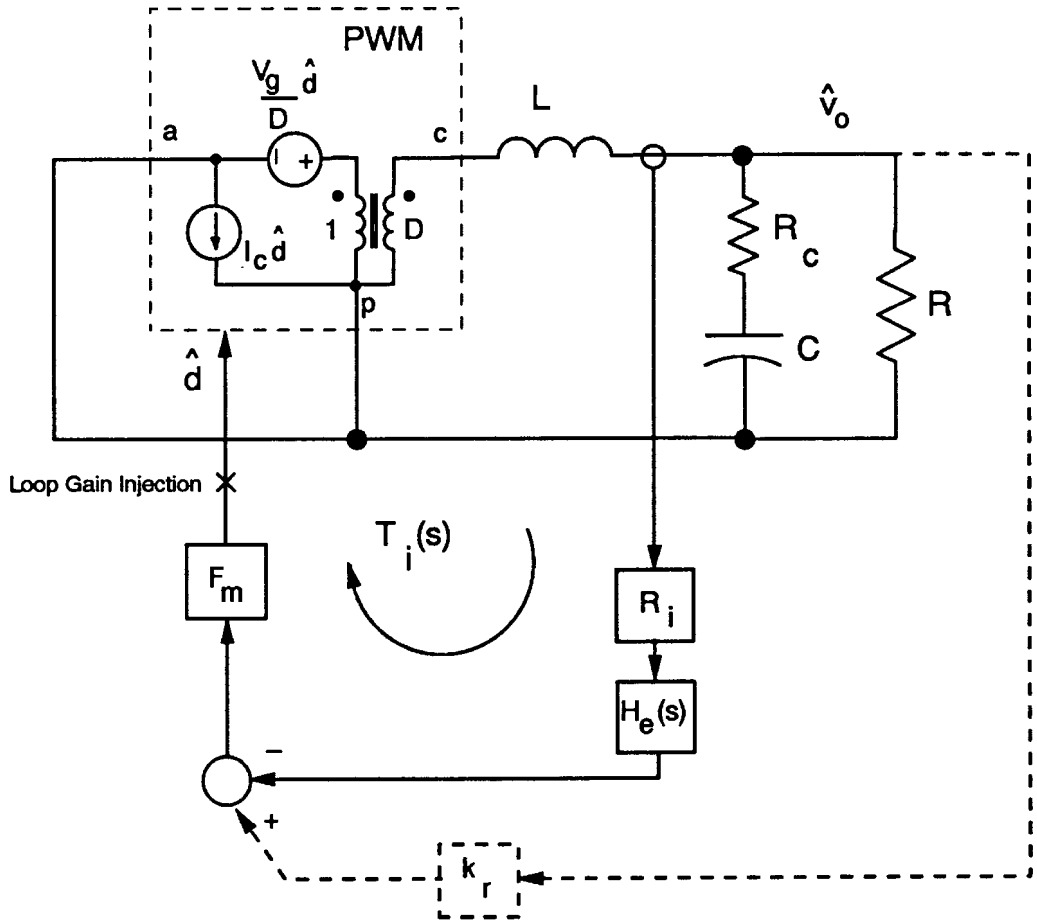


Figure 5.3. ***Current Loop of the Buck Converter:*** *The feedback of the inductor current information creates a closed-loop system, the stability of which can be assessed by examining the current loop gain, $T_i(s)$. This loop gain is measured by breaking the feedback path at the output of the modulator gain, F_m.*

The denominator, $\Delta(s)$, is the power stage transfer function denominator given by the PWM switch model combined with filter components to form the buck converter:

$$\Delta(s) = 1 + \frac{s}{\omega_o Q_{ps}} + \frac{s^2}{\omega_o^2} \tag{5.2}$$

where

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{5.3}$$

and

$$Q_{ps} = \frac{1}{\omega_o\left[\frac{L}{R} + CR_c\right]} \tag{5.4}$$

Like the average models [16-19], the predicted current loop of the new current-mode model has a low-frequency zero, and a double pole at the output filter resonant frequency. Apart from these similarities, the current-loop gain expression of Eq. 5.1 differs significantly from averaged models. The important differences are the dc gain, and the presence of the sampling gain transfer function, $H_e(s)$. The dc gain of the current loop is inversely proportional to the parameter m_c. As more external ramp is added to the system, m_c becomes larger, and the loop gain decreases.

The importance of the sampling gain, $H_e(s)$, is apparent when the current loop gain is plotted. Fig. 5.4 shows plots of the current-loop gain, with different values of external ramp, at a duty cycle of $D = 0.45$. This plot was generated using the model of Appendix B, and includes the effect of the feedback term, k_r. The term $H_e(s)$ introduces a pair of complex RHP zeros, predicted by Eqs. 4.3-4.5 that cause the gain of the loop to become flat at half the switching frequency, and the phase to drop an additional ninety degrees at this point.

The shape of the gain and phase curves do not change with added external ramp. For the case with no external ramp ($m_c = 1$), it can be seen that there is very little gain margin or phase margin in the current loop. If the duty cycle increases further, the gain increases and the system becomes unstable at D = 0.5. Unlike previous average models for current-mode control, the new model completely explains the phenomena for current-loop instability by showing the small phase margin as the instability point is approached. Also, the means by which the external ramp stabilizes the system is accounted for.

An interesting feature of the current loop gain is the high-frequency asymptote of the transfer function. Above the resonant frequency of the power stage, the loop gain is approximated by

$$T_i(s) \simeq \frac{F_s}{m_c D'} H_e(s) \tag{5.5}$$

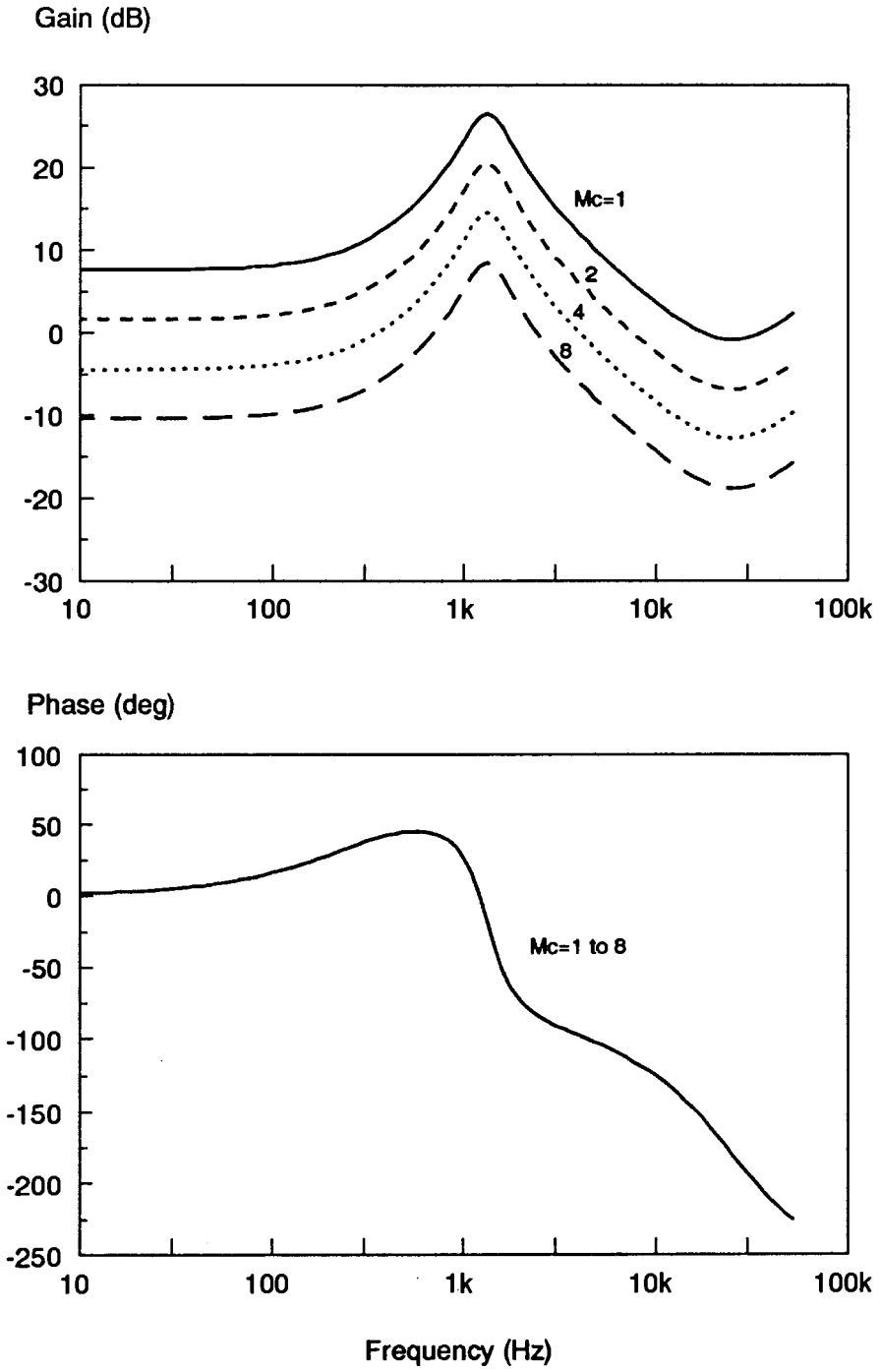


Figure 5.4. ***Buck Converter Current Loop Gain:*** *This figure shows the effect of the RHP zeros of $H_e(s)$ on the current loop stability. At half the switching frequency, the phase of the current loop is -180 degrees, and the system is unstable with too much gain. The gain of the current loop is reduced by adding an external ramp to the system.*

This high-frequency transfer function is actually the same for *all* power stages when constant-frequency control with a clock initiating the on-time is used. This is not surprising since the generic current cell is common to all converters, and the generic cell is the approximate equivalent circuit for finding the inductor current transfer function for all converters above the resonant frequency of the power stage.

A proper average model of the current mode system would produce the same transfer function as Eq. (5.5), with the sampling gain $H_e(s) = 1$.

$$T_i^{ave}(s) \simeq \frac{1}{s} \frac{F_s}{m_c D'} \tag{5.6}$$

This transfer function has the familiar -1 slope of the current feedback with average models [16-19], but has a crossover frequency of

$$f_c = \frac{F_s}{2\pi m_c D'} \tag{5.7}$$

With no external ramp, $m_c = 1$, and the crossover frequency predicted by the average model at a duty cycle of 0.5 is $\frac{F_s}{\pi}$. Hence, using average models, the *maximum* crossover frequency before the system goes unstable is about one-third of the switching frequency. (This was predicted by the model in [20]). Addition of external ramp to the system will reduce this crossover frequency.

This asymptotic crossover differs from predictions of several of the existing average models. For the model in [18], there is a factor of two difference, attributable to different expressions for the modulator gain. In [16], the crossover frequency can be very much higher, depending upon the duty cycle, and value of external ramp used. Of course, no model should predict a crossover frequency in excess of half the switching frequency, since this would exceed the Nyquist frequency. These flaws in earlier models were seldom observed as being severe, however, since most practical applications use an external ramp. When a fairly large external ramp is used, the models of both [16] and [18] will predict approximately the same crossover frequency as the new model.

The characteristics of the current loop gain of the converter show how the external ramp of the system should be selected, based upon the desired phase margin and crossover frequency. However, many designers find it inconvenient to measure the current loop gain of the system, and it is just as straightforward to select the value of the external ramp based upon the control-to-output transfer function predicted by the new model when the current loop is closed. This is discussed in more detail in the next section of this chapter.

Measurements were made on the experimental converter of Fig. 5.2 to confirm the modeling of the current loop gain. It was necessary to increase the input voltage of the experimental converter to 14 V to achieve a duty cycle of 0.45, obtained with the theoretical circuit at 11-V input. Circuit inefficiencies and semiconductor voltage drops, not modeled in the analysis, accounted for the in-

creased input voltage. The approximate transfer function of Eq. 5.1 is dependent on duty cycle, not input voltage, so the change in input voltage does not introduce any discrepancies between measurements and predictions.

The measured and predicted current loop gains for $m_c = 1$ (no external ramp) and $m_c = 2$ are shown in Fig. 5.5. As predicted in Eq. 5.1, the effect of adding external ramp is to reduce the gain of the loop. The phase is not affected by the value of external ramp. Both the gain and phase measurements agreed very well with predictions up to half the switching frequency. It is important to point out that a digital modulator [40,41] was used to measure the loop gain. This ensures that the correct sampled-data loop gain is obtained, and that all the feedback paths created by the current loop are measured. As pointed out in [29], other measurement techniques will not produce the proper measurement of the sampled-data loop gain.

5.2.2 Control-to-Output Gain

The use of a digital modulator to measure the loop gain of the current mode system is inconvenient and usually quite impractical for most converters. The digital modulator requires a complex circuit that modulates the output drive signal from the PWM controller, and injects the signal into the circuit via another driver. This is inconvenient in practical situations, and most designers prefer to work with the control-to-output transfer function. Current-mode control as described

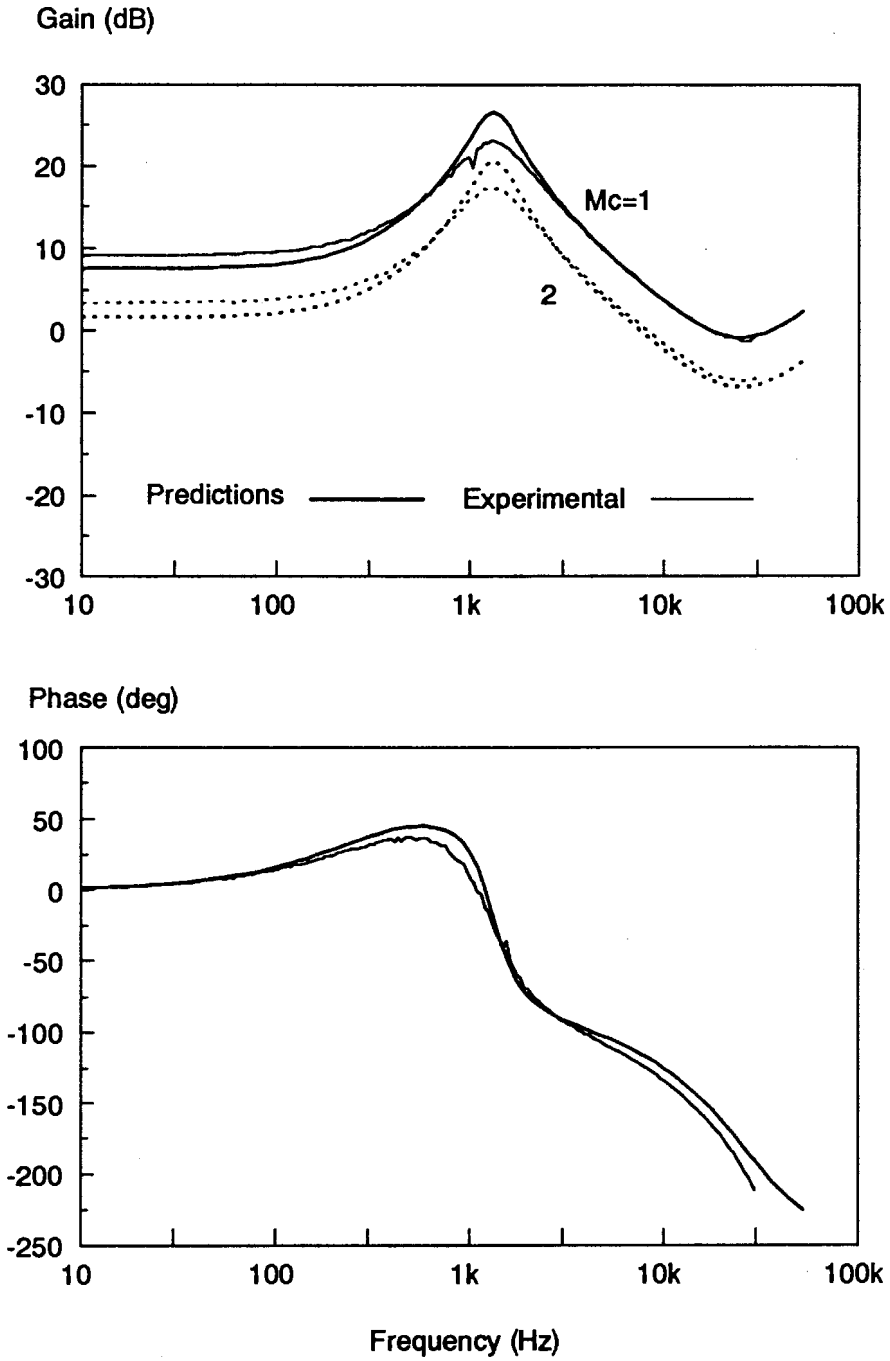


Figure 5.5. ***Buck Converter Current Loop Gain - Experimental Results:*** *The predicted and experimental results for the current loop gain agree very well, especially at higher frequencies where average models fail to predict the current-loop instability.*

in this thesis is implemented with a simple gain in the feedback network. In the absence of any compensation here, the only design freedom in the current loop is to reduce the gain of Eq. (5.1) from a maximum value determined by the operating condition, with $m_c = 1$. The gain is reduced by the addition of an external ramp, as demonstrated in the previous section of this chapter, increasing the value of m_c. In light of the lack of design freedom, it is usually preferable to characterize the effect of the closed current loop from outside the loop.

Fig. 5.6 shows the small-signal model for derivation of the control-to-output transfer function of the buck converter with the current loop closed. The input control parameter is now the voltage $\hat{v}_c$, not the duty cycle of the converter. The closed current loop of the system changes the characteristics of the power stage, and the stability of the current loop can be assessed by looking at the control-to-output transfer function.

The control-to-output transfer function with the current loop closed can be derived from the circuit diagram of Fig. 5.6. If the current loop gain is reasonably high (that is, it has significant gain at the output filter resonant frequency), the expression for the control-to-output transfer function can be approximately factored into a simple form. The approximate control-to-output transfer function for the buck converter with current-mode control is given by

$$\frac{\hat{v}_o}{\hat{v}_c} \simeq \frac{R}{R_i} \frac{1}{1 + \frac{RT_s}{L}[m_c D' - 0.5]} F_p(s) F_h(s) \tag{5.8}$$

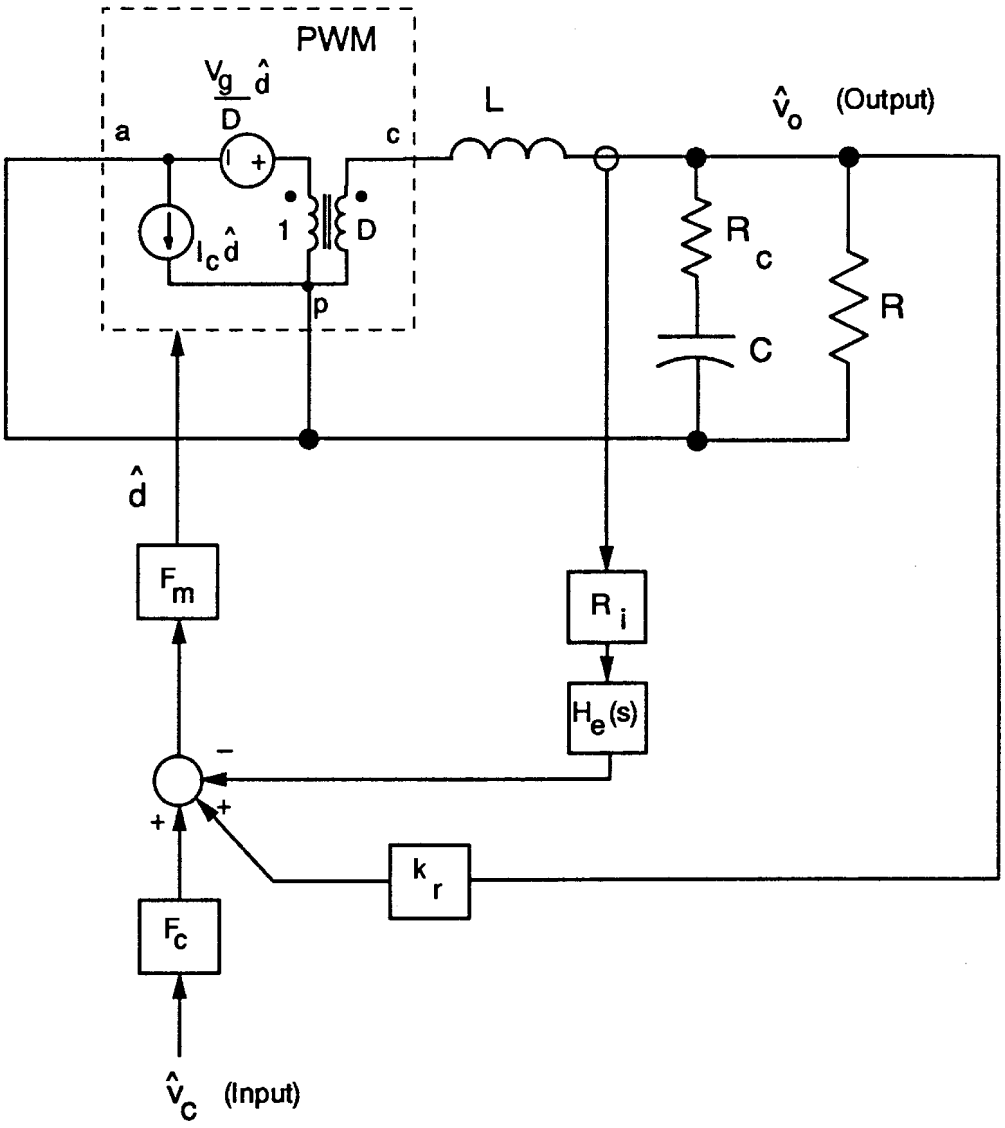


Figure 5.6. ***Buck Converter with Current-Loop Closed:*** *The closed current loop of the system changes the control-to-output characteristics. Most designers prefer to use the control-to-output transfer function to select the closed-loop compensation.*

where

$$F_p(s) = \frac{1 + sCR_c}{1 + \frac{s}{\omega_p}} \tag{5.9}$$

where

$$\omega_p = \frac{1}{CR} + \frac{T_s}{LC}(m_c D' - 0.5) \tag{5.10}$$

and

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}} \tag{5.11}$$

where

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)} \tag{5.12}$$

The transfer function, $F_p(s)$, gives the dominant low-frequency characteristics of the system. For some average models [23,25,26,27] this is the *only* dynamic expression considered for the system, and higher-frequency effects are ignored. Furthermore, the pole location of ω_p, given in Eq. 5.10, is more accurate than that predicted by previous average models [16-27]. The increased accuracy is important in showing how the low-frequency pole moves as less current feedback is used. It is important to see that the low-frequency pole moves to a higher frequency as more external ramp is added to the system.

The transfer function, $F_h(s)$, shows the effects of the sampling action on the system. Notice $F_h(s)$ gives a double pole at half the switching frequency, and the quality factor, Q_p, of this pole pair depends upon the duty cycle of the converter and the added external ramp. This pole pair is produced by the complex RHP zeros in the closed current loop. The small phase margin when the current loop crossover is too high gives a high value for Q_p.

It is important to note that the expression for the high frequency poles given by $F_h(s)$ in Eqs. 5.11-5.12 is the same for *all* power stages with constant frequency control, and the clock initiating the on time. The existence of this pair of complex poles is one of the most significant features of the new current-mode model. The model for the two-state converter system has three poles. This contrasts significantly with previous average models which have two system poles [16-22], one of which is assumed to be at very high frequency in some modeling approaches, or nonexistent in others [24-27]. It will be seen that the presence of the three poles is critical to the accurate modeling of the current-mode system.

Fig. 5.7 shows a set of plots of the control-to-output transfer function of the buck converter, with the current loop closed, for different values of external ramp added to the system. The first curve, with no external ramp added to the system ($m_c = 1$), shows the single-pole response at low frequencies, and the very high-Q peaking of the pair of poles at half the switching frequency. This is for a duty cycle of 0.45, close to the instability point of the current loop. The second curve, with $m_c = 1.2$, shows how the addition of a small amount of external ramp

quickly damps the complex poles, eliminating the instability at half the switching frequency.

Fig. 5.8a shows the pole locations of the system with the current loop closed, with no external ramp added to the system. The poles at half the switching frequency are always complex for this case. At a duty cycle of $D = 0$, they have a Q_p of $\frac{2}{\pi}$, as predicted by Eq. 5.12. As the duty cycle increases towards $D = 0.5$, these poles move towards the imaginary axis, becoming purely imaginary with a $Q_p = \infty$ at $D = 0.5$, and the poles move into the right-half plane for higher duty cycles. (For constant-frequency control, with *leading* edge modulation, the poles would have a $Q_p = \frac{2}{\pi}$ at a duty cycle of 1, and be in the right-half plane for duty cycles *less* than 0.5.)

Fig. 5.8b shows the effect of an external ramp on the system with a duty cycle of $D = 0.45$. As an external ramp is added to the system, the poles move closer to the real axis, eventually splitting into two real poles. One of these poles then moves out to high frequencies, and the other moves in towards the resonant frequency of the power stage. When sufficient external ramp is added to the system to reduce the current loop gain to a point where the gain at the resonant frequency is less than 1, this pole combines with the low-frequency pole of $F_p(s)$ in Eq. (5.9), to provide the resonant-frequency poles characteristic of voltage-mode control. This is the limiting case for the accuracy of the expression of Eq. 5.8. From the current loop gain plots of Fig. 5.4, this limiting case is with a value of $m_c = 8$ at a duty cycle of $D = 0.45$.

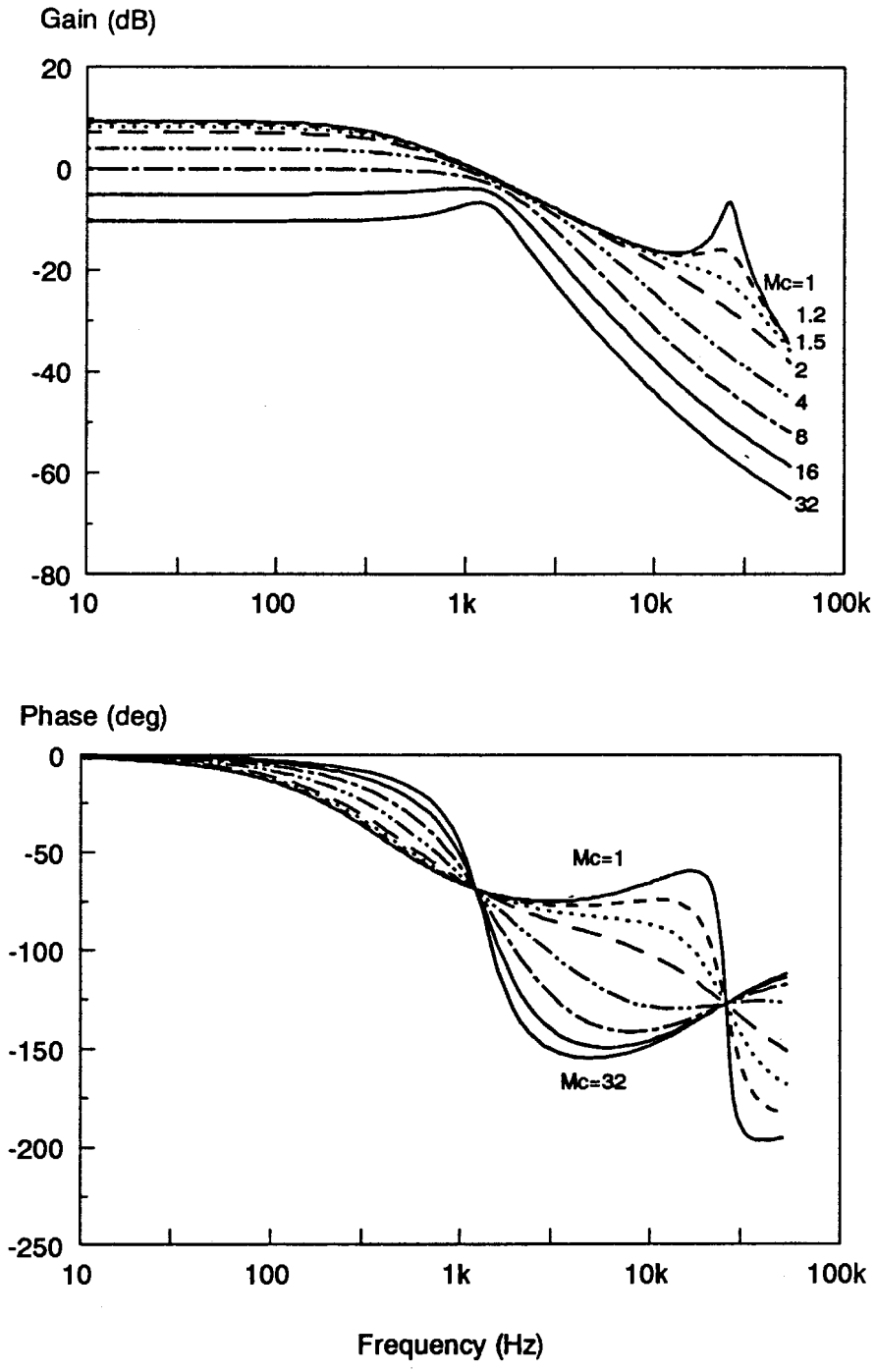
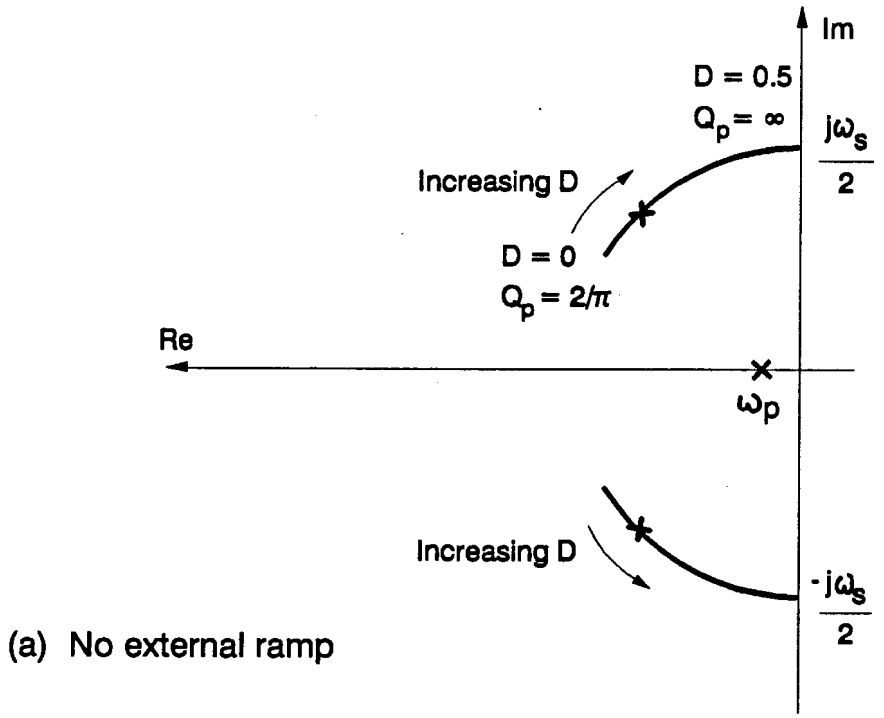
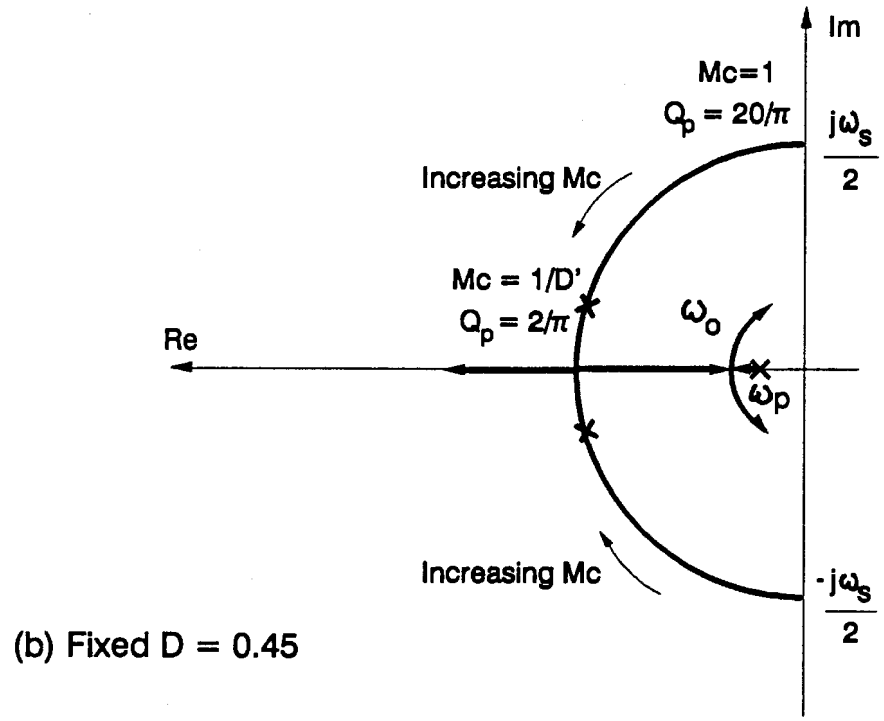


Figure 5.7. ***Control-to-Output Transfer Function with Current-Loop Closed:*** *The low phase margin in the current loop of the system with small external ramp is manifested in the control-to-output transfer function by a pair of complex poles at half the switching frequency. The Q of these poles is controlled by the addition of the external ramp.*



(a) No external ramp



(b) Fixed D = 0.45

Figure 5.8. ***Poles of the System with the Current-Loop Closed:*** *Unlike average current-mode models, the new current-mode model gives a control-to-output transfer function with three poles.*

Figs. 5.7 and 5.8 show the power of the new small-signal model. For the first time, a comprehensive model is given which shows the high-frequency dynamics of current-mode control, yet which also will show the transition from current-mode to voltage-mode control as more external ramp is added to the system. This is very important for modeling purposes: a single model can be used for the two types of control. Separate current-mode and voltage-mode models are not required.

Another important feature of the new model is the simple form of the expressions for the high-frequency dynamics, given in Eqs. (5.11-5.12). This makes the system performance simple to predict and design, and also shows how the system can become unstable when the voltage loop is closed. The instability at half the switching frequency is not just a function of the current loop. It is quite possible for the closed current loop to be stable, but the system can then oscillate when the outer voltage feedback loop is closed. Fig. 5.9 shows the buck converter with a compensation network in the feedback loop from the output voltage. To demonstrate how the feedback loop can cause the current-loop instability, an integral-and-lead network is assumed.

The converter of Fig. 5.9 is operating at a duty cycle of $D = 0.45$. From Eq. (5.12) this produces a pole pair in the control-to-output transfer function at half the switching frequency, with $Q_p = \frac{20}{\pi}$. The system is stable with the current loop closed. When an integrator and lead network is added to the control loop feedback from the output voltage, the loop gain shown in Fig. 5.10 results. This

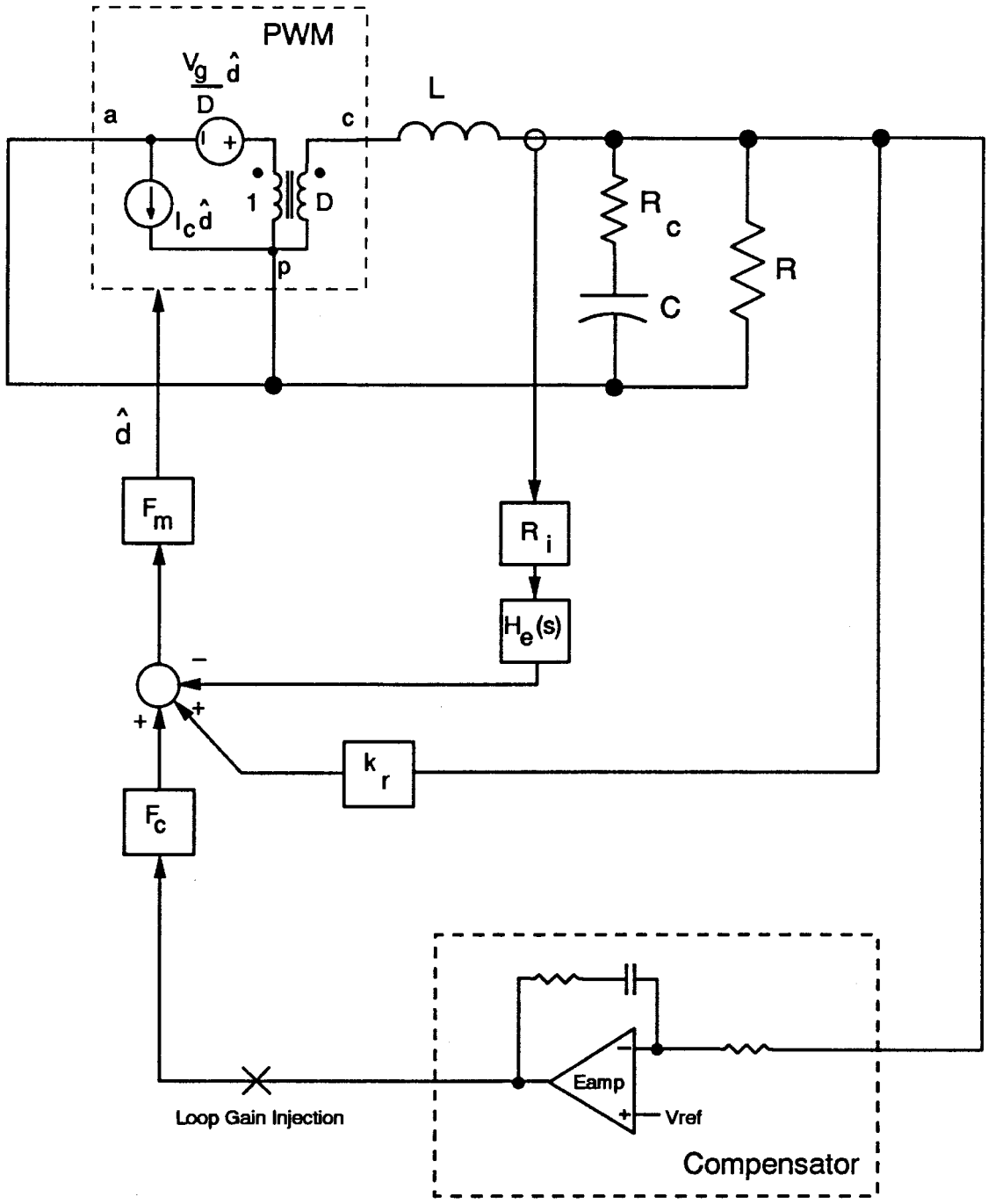


Figure 5.9. ***Buck Converter with Feedback Compensator and No External Ramp:*** *With no external ramp, addition of a compensation network can cause the previously-stable current loop to oscillate. The loop gain of this system, measured at the output of the compensator, shows the cause of the instability.*

loop gain can be measured at the output of the compensator shown in Fig. 5.9. Even though the loop gain has good phase margin at the initial crossover frequency of about 5 kHz, the high-Q poles at half the switching frequency cause the gain to rise above 0 dB again, and the sharp drop in the phase at this frequency causes the system to oscillate at half the switching frequency.

The simple form of the new current-mode model makes it a simple design procedure to avoid current-feedback instability. The approximate control-output transfer function is very useful for design purposes. Eq. (5.12), which holds for all converters, allows suitable choice of external ramp to prevent peaking at half the switching frequency. Choosing a value of $Q_p = 1$ will achieve this, and the required external ramp for all converters is given by

$$m_c = \frac{\frac{1}{\pi} + 0.5}{D'} \tag{5.13}$$

Of course, choosing $Q_p = 1$ is not the only possibility. Other values may be preferable, depending upon the performance parameters to be optimized for a given converter. For example, very low line-to-output noise may be required, and this can be achieved with different values of external ramp for the buck converter, as discussed in the next section of this chapter. Lower values of Q_p may be desirable for systems with addition zeros in the control-to-output transfer function. Design strategies can be used where a large external ramp is added to split the

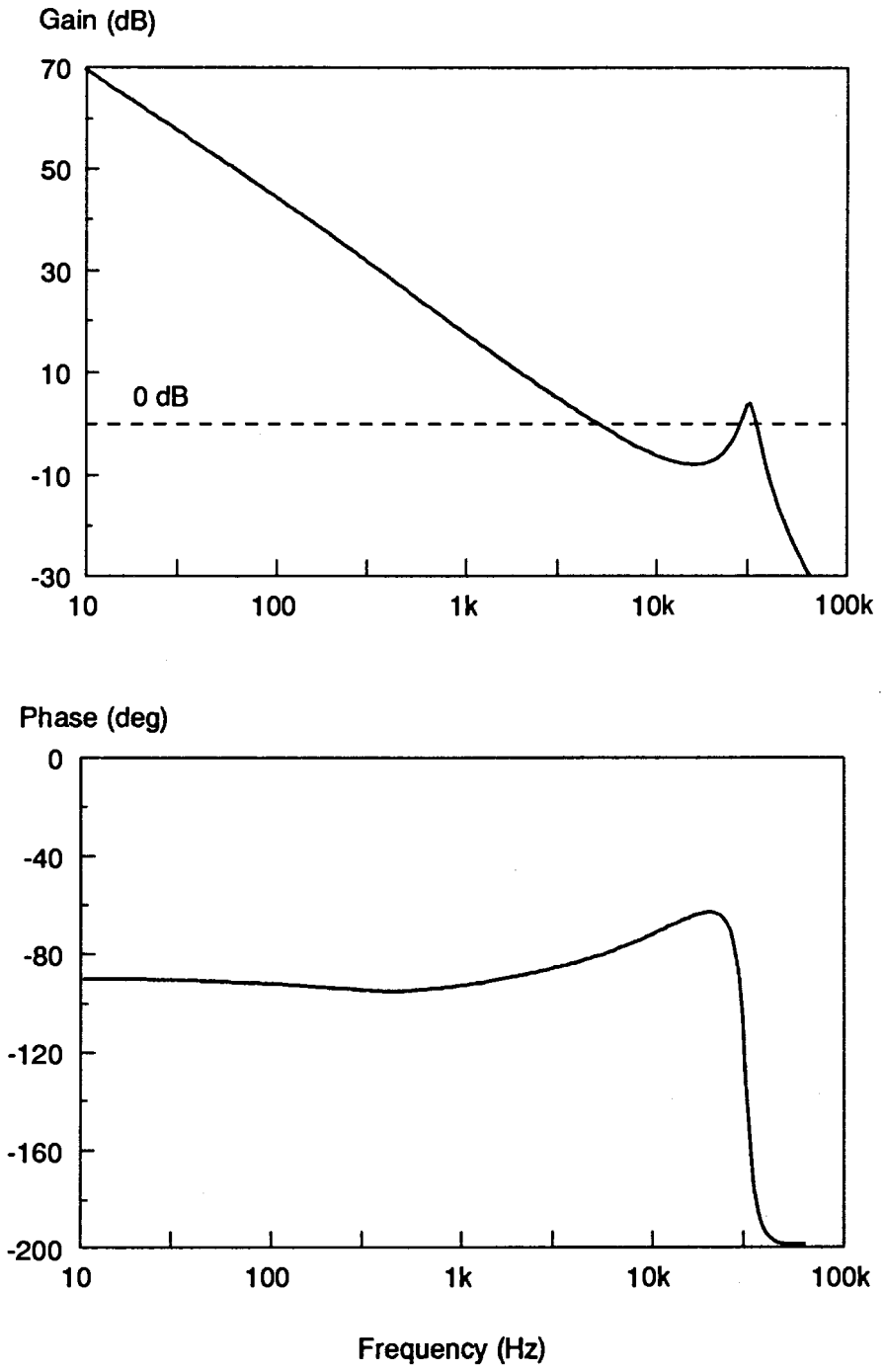


Figure 5.10. ***Loop Gain of Buck Converter without an External Ramp:*** *If the high-Q poles of the system are not damped with an external ramp, introduction of outer-loop feedback can make the system unstable, even at duty cycles considerably less than 0.5.*

double pole, and use one of them to cancel a zero of the control-output transfer function.

Fig. 5.7 highlights one of the biggest benefits of current-mode control. If the phase of the control-to-output transfer function with a value of $m_c = 1.5$ is compared to that of the curve with $m_c = 32$ (approximating voltage-mode control) the substantial increase in phase is apparent. In the region of 5-10 kHz, where a good performance control loop would be crossed over, the current-mode system has over 50 degrees improved phase. This allows a simpler compensator to be used for current-mode control systems.

Fig. 5.11 shows the comparison between theoretical results predicted by the new model, and experimental results obtained from the circuit of Fig. 5.2. The agreement between the measured and experimental results is excellent, even beyond half of the switching frequency. The peaking of the poles at half the switching frequency is very accurately predicted and matched by the measurements. Limits on the maximum input of the current mode modulator of the UC3825 control chip prevented the value of m_c from being increased beyond 4.

5.2.3 Audio Susceptibility Transfer Function

The audio susceptibility of the buck converter shows one of the most interesting properties of current-mode control, and this is one of the motivations for selecting

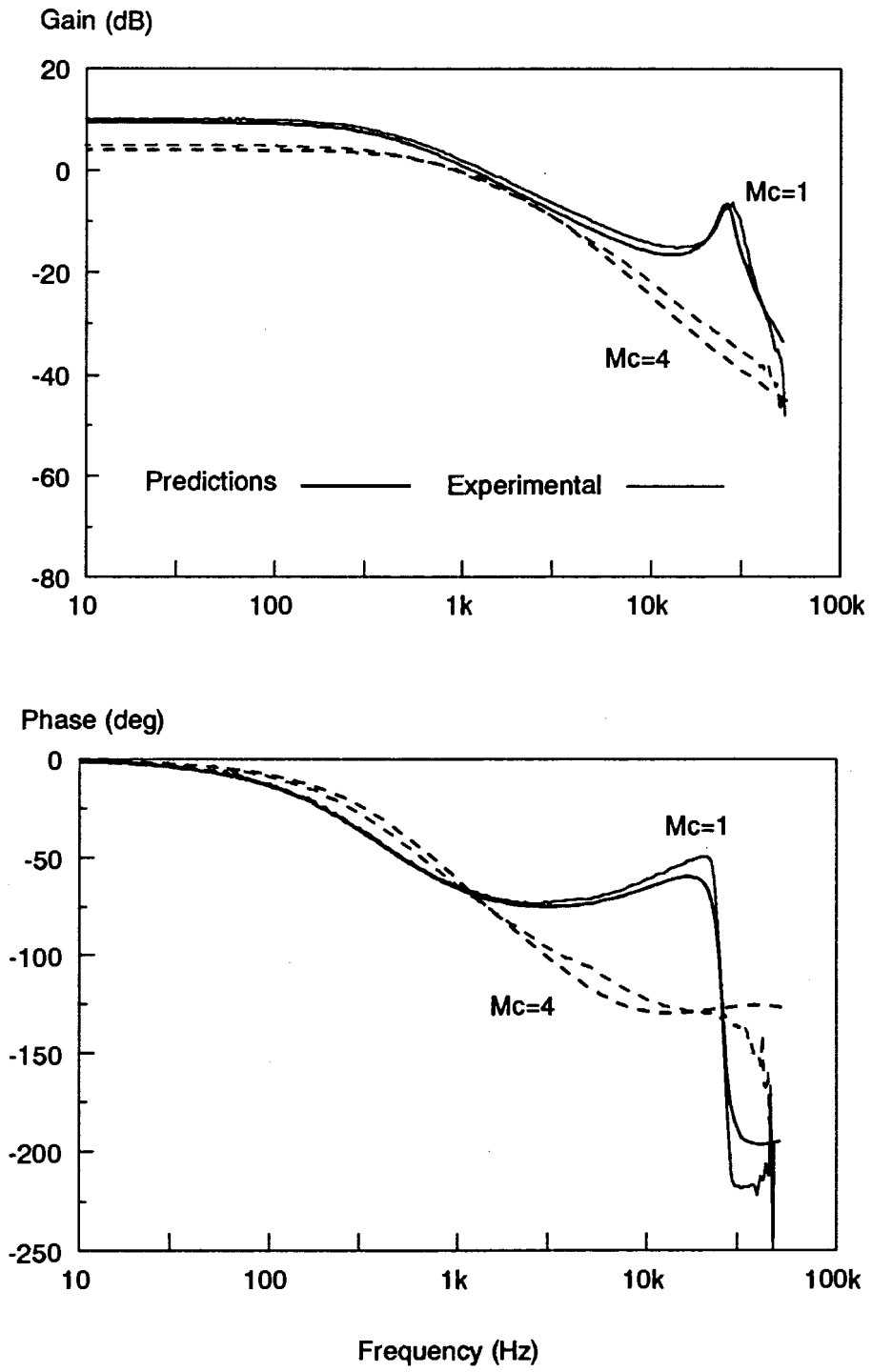


Figure 5.11. ***Control-to-Output Transfer Function - Experimental Results:*** *The very high Q with no current ramp was accurately predicted by the model, and matched by the experimental results. Increase of the parameter m_c beyond a value of 4 was impractical on the experimental converter due to the limited supply voltage to the current-mode comparator. Larger values of m_c require too large an external ramp.*

this converter as an example of the application of the new current-mode control model. Fig. 5.12 shows the buck converter model with perturbations in the input voltage. Notice that the input voltage perturbations are fed into the power stage by two mechanisms. One is through the small-signal model of the power stage itself, where the input source, $\hat{v}_g$, is connected to the small-signal 1:D transformer. A second path is through the control network, into the duty cycle perturbation, $\hat{d}(s)$, via the feedforward gain term, k_f. The feedforward term is negative, and since the controlled source is connected in series with the input voltage source in the small-signal model, it is possible to have conditions in the circuit where the net effect of input-voltage perturbations on the output of the small-signal model is zero. Perturbations at the input of the power stage are cancelled out by equal and opposite perturbations due to the feedforward of the input voltage through the control system.

The circuit of Fig. 5.12 allows the expression for the audio susceptibility to be derived. Assuming that the current-loop has significant gain at the resonant frequency of the output filter, the transfer function can then be approximately factored. The resulting approximate audio transfer function for the buck converter is

$$\frac{\hat{v}_o}{\hat{v}_g} = \frac{D[m_c D' - (1 - D/2)]}{\frac{L}{RT_s} + (m_c D' - 0.5)} F_p(s) F_h(s) \tag{5.14}$$

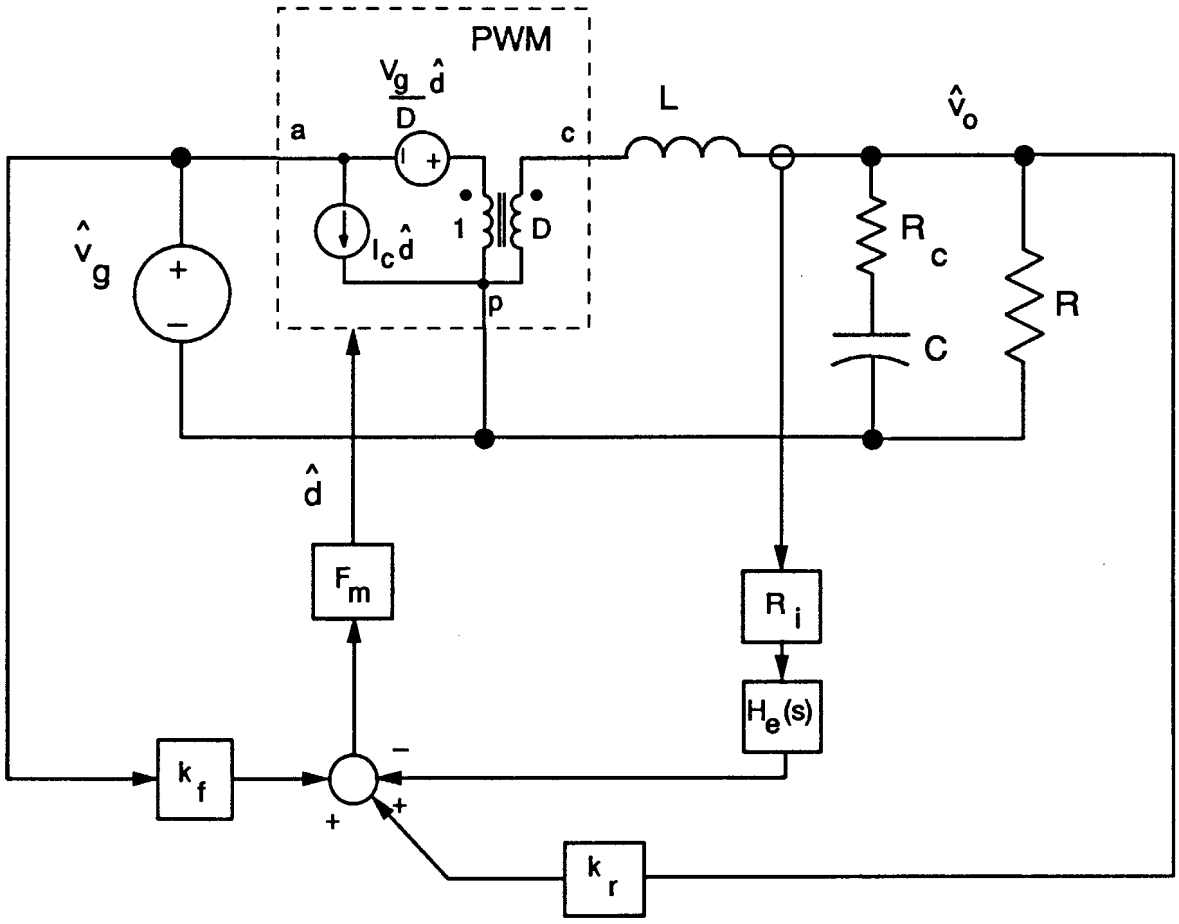


Figure 5.12. ***Converter System with Current-Loop Closed and Input Perturbation:*** *Closing the current loop has a profound effect on the line-to-output transfer function, due to the gain of the current loop, and the feedforward term, k_f.*

where $F_p(s)$ and $F_h(s)$ are given in Eqs. (5.9-5.12). Notice that the numerator of the dc gain of this expression is a difference of two terms. This shows the possibility of nulling the audio susceptibility of the buck converter with suitable control design and power stage parameters.

Fig. 5.13 shows a series of plots of audio susceptibility for different values of external ramp. The curve with $m_c = 1$ corresponds to no external ramp in the system, and the curve with $m_c = 32$ corresponds to a very large external ramp, approximating the characteristics of a voltage-mode system.

With no external ramp, the transfer function shows the same dominant pole of the control-to-output transfer function, and a pair of high-Q complex poles at half the switching frequency. Notice that the audio susceptibility is considerably reduced at most frequencies compared to that of voltage mode control ($m_c = 32$). This is an important advantage of current-mode control.

As external ramp is added to the system, the audio susceptibility of the buck converter is reduced, even though the current feedback loop gain, shown in Fig. 5.4, is decreased. This is due to the nulling effect of the feedforward term, k_f. Addition of external ramp also damps the peaking of poles at half the switching frequency.

The decrease in the audio susceptibility continues with further addition of ramp until the null value of ramp is reached. The null in audio susceptibility occurs

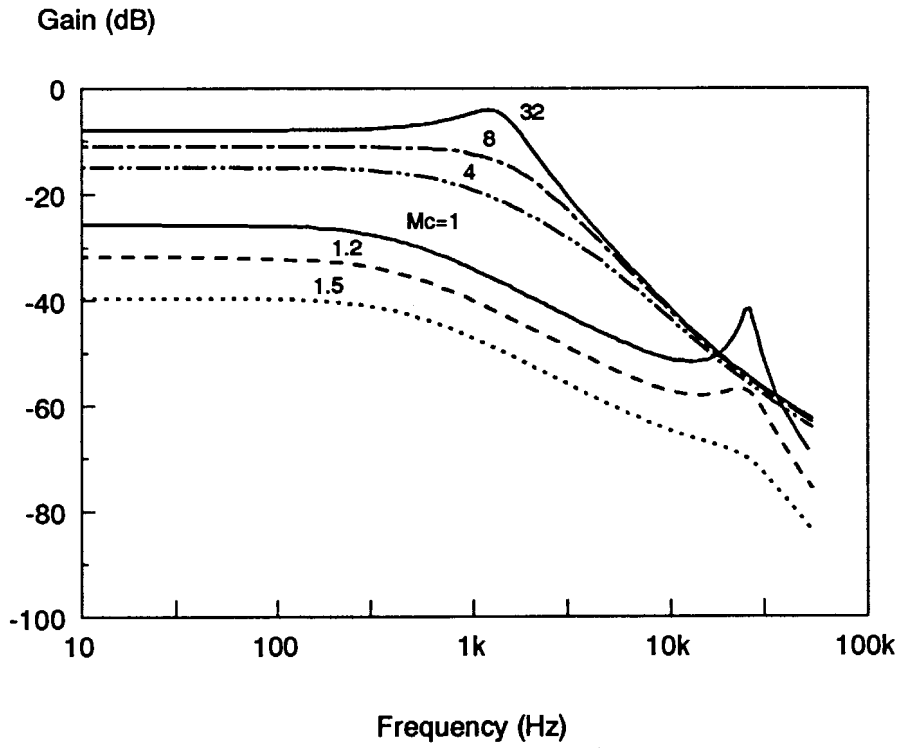


Figure 5.13. ***Line-to-Output (Audio Susceptibility) of the Buck Converter:*** *The audio susceptibility of the buck converter has the interesting feature of a null value for the critical value of external ramp. As the external ramp is increased through the null value, the phase of the audiosusceptibility changes sign.*

with an external ramp value $S_e = S_f/2$. This null value is also predicted by the average model of [18] which also had a feedforward term (although different from that found in this dissertation), and predicted, with some waveform discussion, in [23]. Average models [5,6,16] without the feedforward term fail to show the nulling effect.

Choosing the external ramp to null the audio susceptibility can be useful for applications where output noise is extremely critical. However, the audio susceptibility is very sensitive to changing values of the external ramp around this null value, and it can be difficult obtain a precise null. It can be seen from the curves of Fig. 5.13 that small changes in the value of the external ramp cause relatively large changes in the audio susceptibility around the null value.

At values of external ramp less than the critical value, it is interesting to note that the audio susceptibility transfer function starts with a phase of -180 degrees at dc. An increase in the dc value of the input voltage of the converter causes a *decrease* in the output voltage when the current loop is closed with a small external ramp. The reason for this is clearly demonstrated by the waveforms of Fig. 5.14. As the input voltage is increased, the peak current is regulated to a constant value in the case with no external ramp. The current ripple of the converter increases with the higher input voltage, and hence the average current of the converter (given by the peak current minus half the ripple current) decreases.

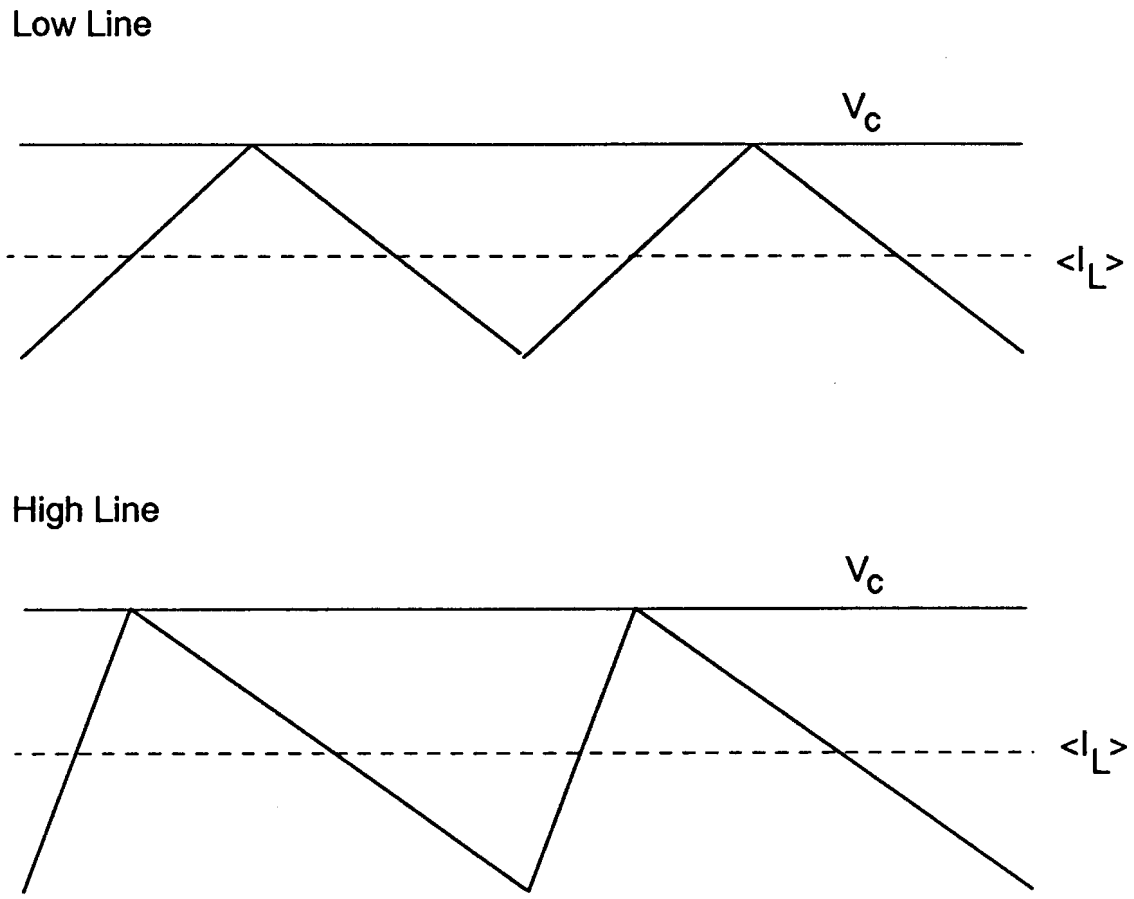


Figure 5.14. ***Steady-State Waveforms of the Buck Converter with No External Ramp:*** *As the input line is increased, the steady-state ripple current is also increased. Since the peak of the current is regulated, the average value of the current, and hence the output voltage, is decreased.*

The experimental measurements of audio susceptibility are shown in Fig. 5.15. The theory and experiment agree very well with no external ramp, but measurements were difficult to obtain as the audio susceptibility became lower with more external ramp. Higher frequency measurements below -55 dB were unreliable, due to noise and grounding problems. However, the nulling effect of the external ramp was experimentally verified, with the audio susceptibility decreasing to a very low minimum value, then increasing with more external ramp. The measurements were extremely sensitive around the value $m_c = 1.5$, with small variations in the ramp causing large changes in the audio susceptibility. The dc phase of the audio measurement, not shown in this figure, changed from -180 degrees to zero degrees as the external ramp increased through its null value.

5.2.4 Output Impedance Transfer Function

The output impedance of the buck converter with the current loop closed can be derived from the circuit model of Fig. 5.16. The input-voltage perturbation in this figure is zero, and feedforward gain, k_f, is not needed. Perturbations in the duty cycle, $\hat{d}$, are produced by feedback of the inductor current, and the output voltage, via k_r. The input perturbation to the circuit is produced by a small-signal current source, $\hat{i}_o(s)$, applied at the output of the converter. The resulting output impedance transfer function for the buck converter is

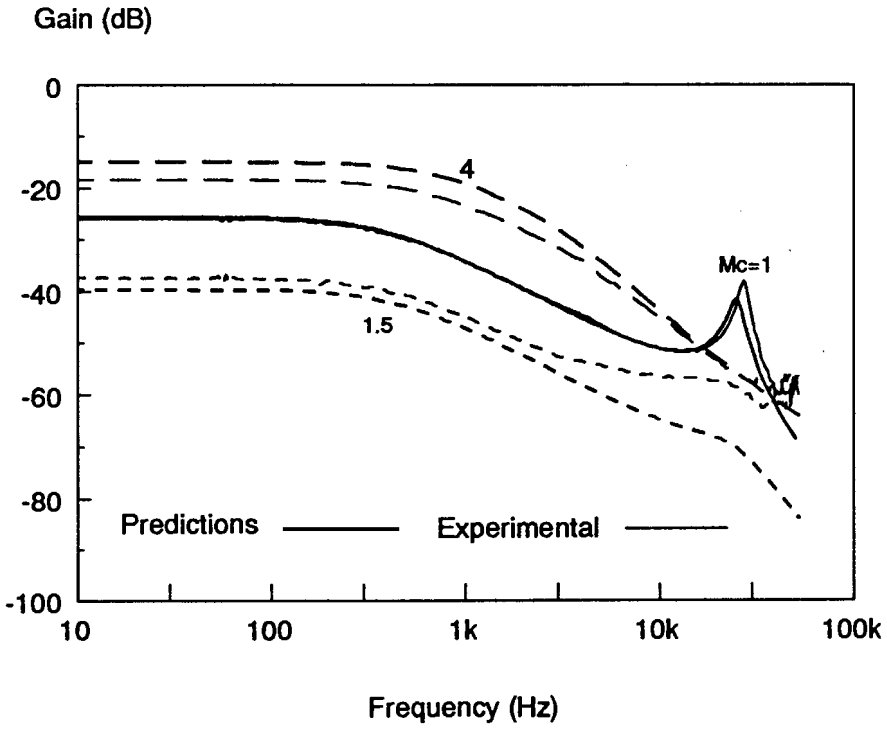


Figure 5.15. ***Audiosusceptibility of the Buck Converter - Experimental Results:*** *Experimental measurements confirm the existence of the null value of the audiosusceptibility, although readings below the circuit noise level could not be attained. The measurements in the region of the null are very sensitive to any small changes in the slope of the external ramp.*

$$Z_o(s) \simeq \frac{R}{1 + \frac{RT_s}{L}(m_c D' - 0.5)} F_p(s) \qquad (15)$$

where $F_p(s)$ is given by Eqs. (5.9-5.10). This expression is accurate when the current loop has considerable gain at the output filter resonant frequency.

With small ripple current in the converter (i.e. with large L or small switching period, T_s) the low-frequency value of the output impedance is approximately the dc load resistance, R, agreeing with simple average models. The transfer function for the output impedance has the same dominant pole as the control-to-output transfer function, and a zero due to the ESR corner frequency of the output filter capacitor. The second-order poles at half the switching frequency do not appear in this transfer function.

Closing the current feedback loop has a strong effect on the output impedance of the converter. Fig. 5.17 shows the output impedance of the buck converter with increasing values of m_c. The curve with $m_c = 1$ is without any external ramp, and the curve with $m_c = \infty$ corresponds to voltage-mode control. Even with high values of m_c, and correspondingly low levels of current feedback, there is a significant effect on the low-frequency asymptote and damping of the LC-filter resonance. This effect on the low-frequency output impedance is the one potential drawback of current-mode control. The natural voltage-source characteristics of voltage-mode control, where the output voltage is relatively insensitive to load current, are not retained. Feedback of the inductor current cre-

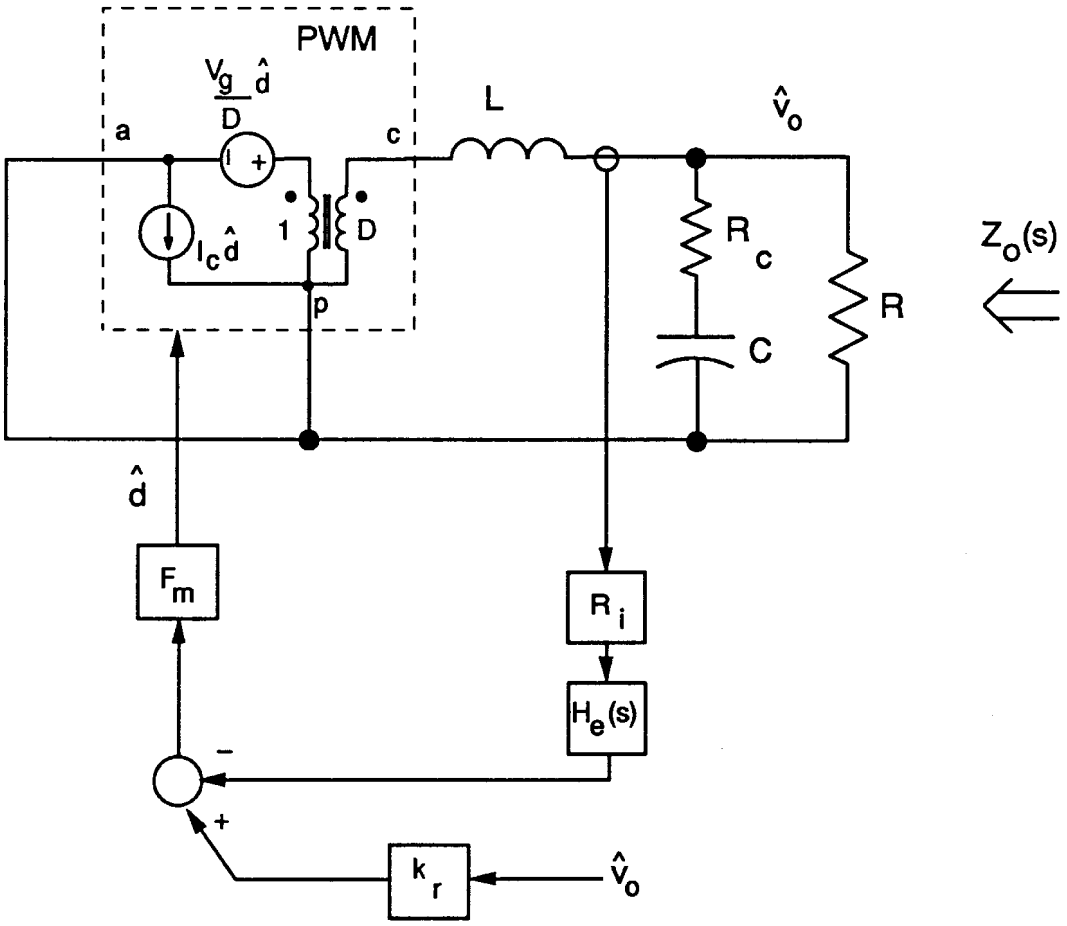


Figure 5.16. ***Converter System with Current-Loop Closed and Load Current Perturbation:*** *The closed current loop will maintain the peak value of the current constant, and the output impedance is increased in the presence of current-mode control.*

ates a soft current source, and a corresponding increase in impedance. Fortunately, high feedback gain from the output voltage can usually be used in the system to attenuate the final output impedance to a very low value.

The measured and predicted output impedance, shown in Fig. 5.18, agreed well with external ramp added to give values of m_c from 1 to 4.

5.3 Constant Off-Time Control in CCM

5.3.1 Current-Loop Gain

The model for the constant off-time control is very similar to that of constant-frequency control, with two significant differences. Firstly, although the current loop dynamics of the constant frequency and constant off-time converter are the same, the gain of the modulator in the current-loop, given in Eq. 3.21 is different. The gain of the current loop of Fig. 5.4 was derived for the constant frequency case to be

$$T_i(s) \simeq \frac{L}{RT_s m_c D'} \frac{1 + sCR}{\Delta(s)} H_e(s) \tag{5.16}$$

This is a restatement of Eq. (5.1). It was shown earlier that this transfer function predicts instability when circuit conditions cause a crossover frequency at half the

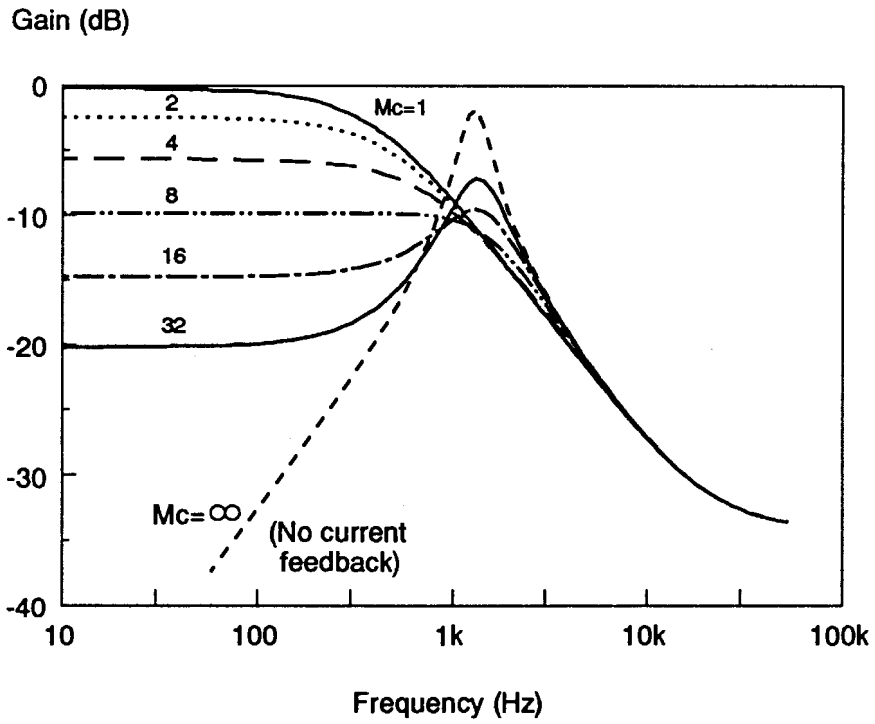


Figure 5.17. ***Output Impedance of the Buck Converter:*** *Closing the current loop has the effect of increasing the output impedance of the converter below the resonant frequency of the filter. This is due to the tendency of the converter to maintain a fixed current when current-mode control is used. Adding an infinite external ramp reduces the current gain to zero, showing the voltage-mode characteristics of the power stage.*

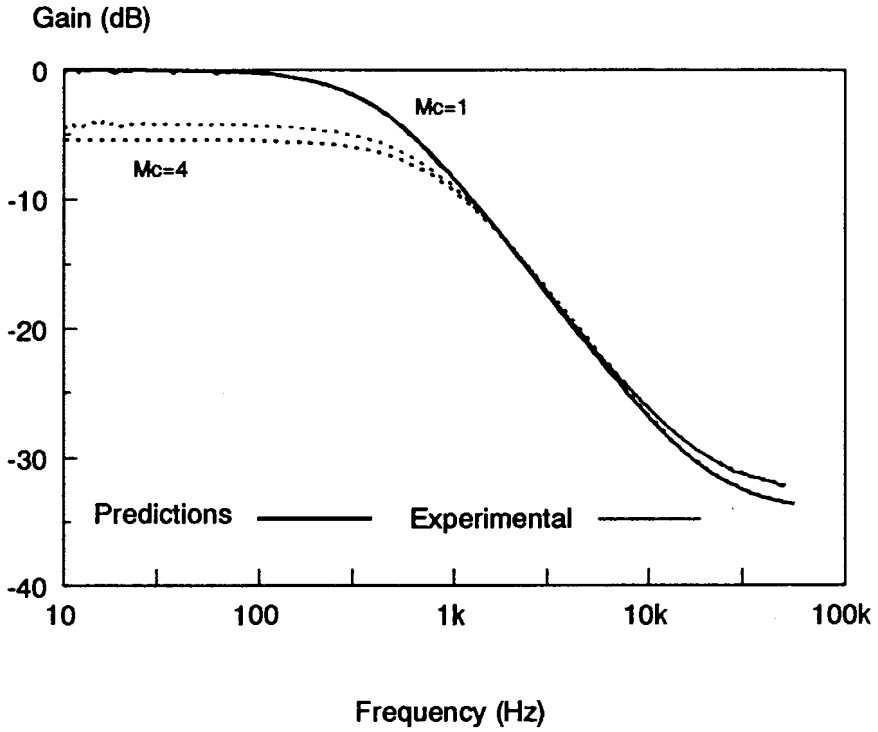


Figure 5.18. Output Impedance of the Buck Converter - Experimental Results: Experimental and predicted measurements agree well.

switching frequency or higher. The modulator gain of the constant-frequency converter was found in Chapter 4 to be

$$F_m = \frac{1}{S_n m_c T_s} = \frac{1}{S_n T_s} \quad \text{with no external ramp} \tag{5.17}$$

The corresponding modulator gain of the constant off-time system without an external ramp was found to be

$$F_m = \frac{D'}{S_n T_s} \tag{5.18}$$

It can be seen that the gain of the constant off-time modulator is a factor D' smaller. This smaller gain is directly reflected in the expression for the current loop gain for constant off time:

$$T_i(s) \simeq \frac{L}{RT_s} \frac{1 + sCR}{\Delta(s)} H_e(s) \tag{5.19}$$

An interesting feature of this transfer function is that it is independent of the operating conditions of the converter. This is unlike the constant-frequency converter which had a gain inversely proportional to the complement of the duty cycle.

A constant off-time control scheme was built for the buck converter described earlier with a duty cycle of $D = 0.45$. This was done by using the UC3825 output

of Fig. 5.2 to trigger a one-shot network which timed the constant off-time, and reset the timing ramp on pin 6 of the controller. The off-time pulse width was adjusted to provide a switching frequency of 50 kHz, allowing comparisons with the constant-frequency converter measurements presented earlier.

The difference in gain of the current loops of the constant-frequency and constant off-time control schemes can be eliminated by adding an external ramp to the constant-frequency control. The value of the ramp added should be equal to the downslope of the sensed inductor current. Fig. 5.19 shows the results of the measured current loop gains of the constant-frequency converter with this value of external ramp, and the constant off-time converter. Both the gain and phase results are identical, confirming the model of the current loop with the constant off-time control. Changes in the operating duty cycle of the constant off-time converter do not affect the measurements presented in Fig. 5.19.

The current loop does not increase its crossover frequency with duty cycle, and it can never exhibit the subharmonic oscillations associated with constant frequency control. (Strictly speaking, the constant off-time converter *can* be made unstable if a *negative* external ramp is added, with a slope equal in magnitude to the sensed current downslope. A small negative ramp can be created by inaccuracies in current-sensing networks, but a properly designed circuit would not do this.) The natural stability of the constant off-time control scheme make it preferable to some researchers [37] over the constant-frequency schemes.

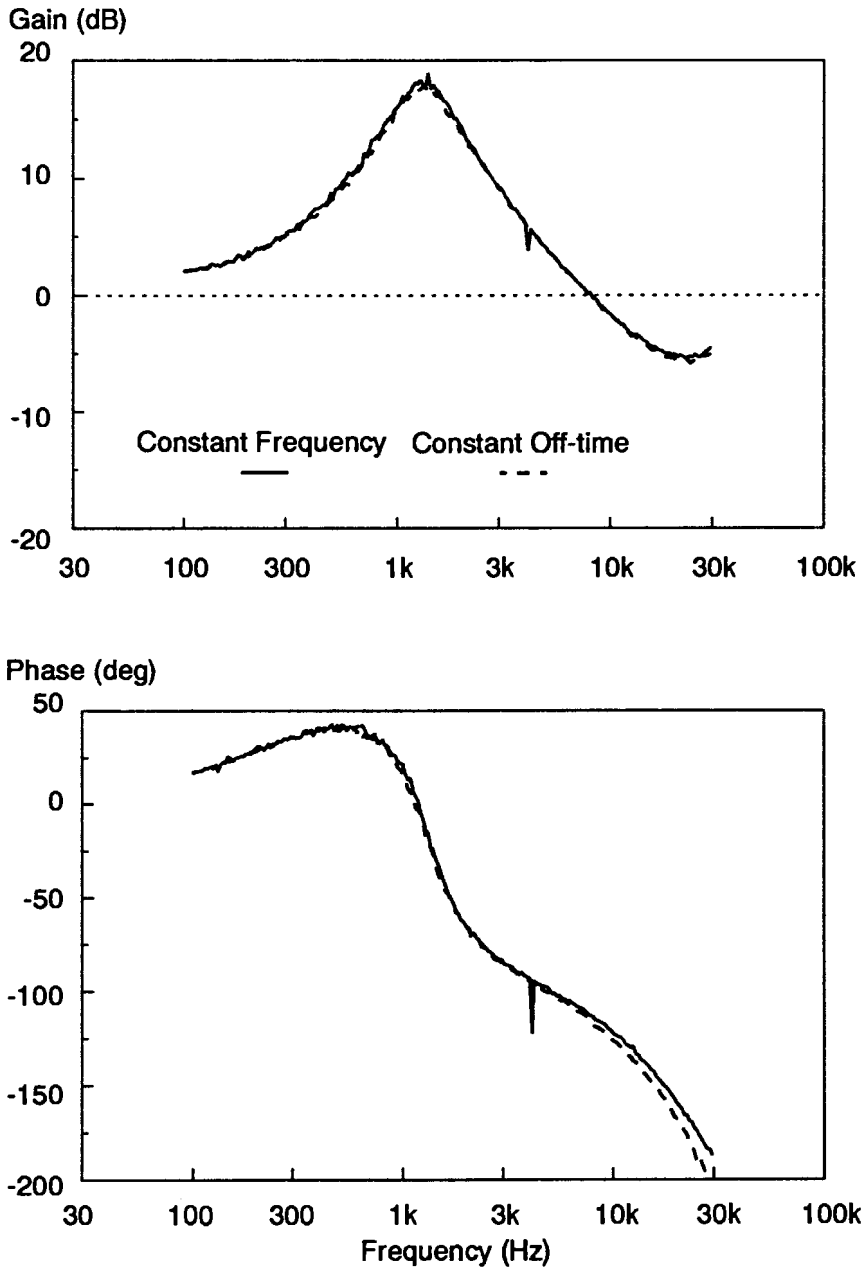


Figure 5.19. ***Current Loop-Gain Measurement for Constant Off-Time:*** *The current loop gain for the constant off-time system is identical to the current-loop gain with constant-frequency control with an external ramp equal to the off-slope of the current signal. This loop gain remains invariant with duty cycle for the constant off-time control, remaining stable under all conditions.*

5.3.2 Control-to-Output Gain

It was shown earlier that the small phase margin of the current loop gain was seen in the control-to-output gain in the form of a pair of poles at half the switching frequency. The Q_p of these poles, given in Eq. 5.12, was a function of the operating conditions of the power supply, and the value of external ramp added.

The current loop gain of the constant off-time system was shown to be invariant with duty cycle, and an external ramp is not needed for stability. Furthermore, it was shown that the current loop gain of the constant off-time system is exactly equal to that of the constant frequency system with an external ramp equal to the downslope of the sensed inductor current. This ramp value can be expressed as

$$S_e = S_f = \frac{D}{D'} S_n \tag{5.20}$$

The value of the ramp parameter, m_c, for this condition is then

$$m_c = 1 + \frac{S_e}{S_n} = 1 + \frac{D}{D'} = \frac{1}{D'} \tag{5.21}$$

The damping of the poles at half the switching frequency was derived in Eq. 5.12. Substituting the value of external ramp parameter found above, a *fixed* value of quality factor, Q_p, is found

$$Q_p = \frac{2}{\pi} \tag{5.22}$$

The fixed value of the quality factor of these poles again illustrates the reason for the stability of the constant off-time controller.

The only difference in the control-to-output response of the constant frequency converter with the appropriate value of external ramp, and the constant off-time converter is due to the modulator phase term, F_c, in Fig. 4.5. For constant frequency control, this term was unity. For constant off-time control, this term shows a phase lead, proportional to the duty cycle and the switching frequency. With duty cycles close to zero, the phase lead is negligible at frequencies up to half the switching frequency. With duty cycles close to unity this term gives almost ninety degrees phase lead at half the switching frequency.

The control-to-output was measured for the two control schemes at a duty cycle of $D = 0.1$, and the results are plotted in Fig. 5.20. The gain of the two curves are almost identical, showing the same dominant pole, given by Eq. 5.9, and the double pole at half the switching frequency with the same quality factor. The phase of the transfer functions does differ slightly due to the small phase lead (about 5°) of the constant off-time modulator.

Figs. 5.21 and 5.22 give circuit predictions and measurements, showing how the new model for constant off-time control accurately predicts the phase lead due to the modulator The duty cycle for the plots of Fig. 5.21 was $D = 0.1$, and that for

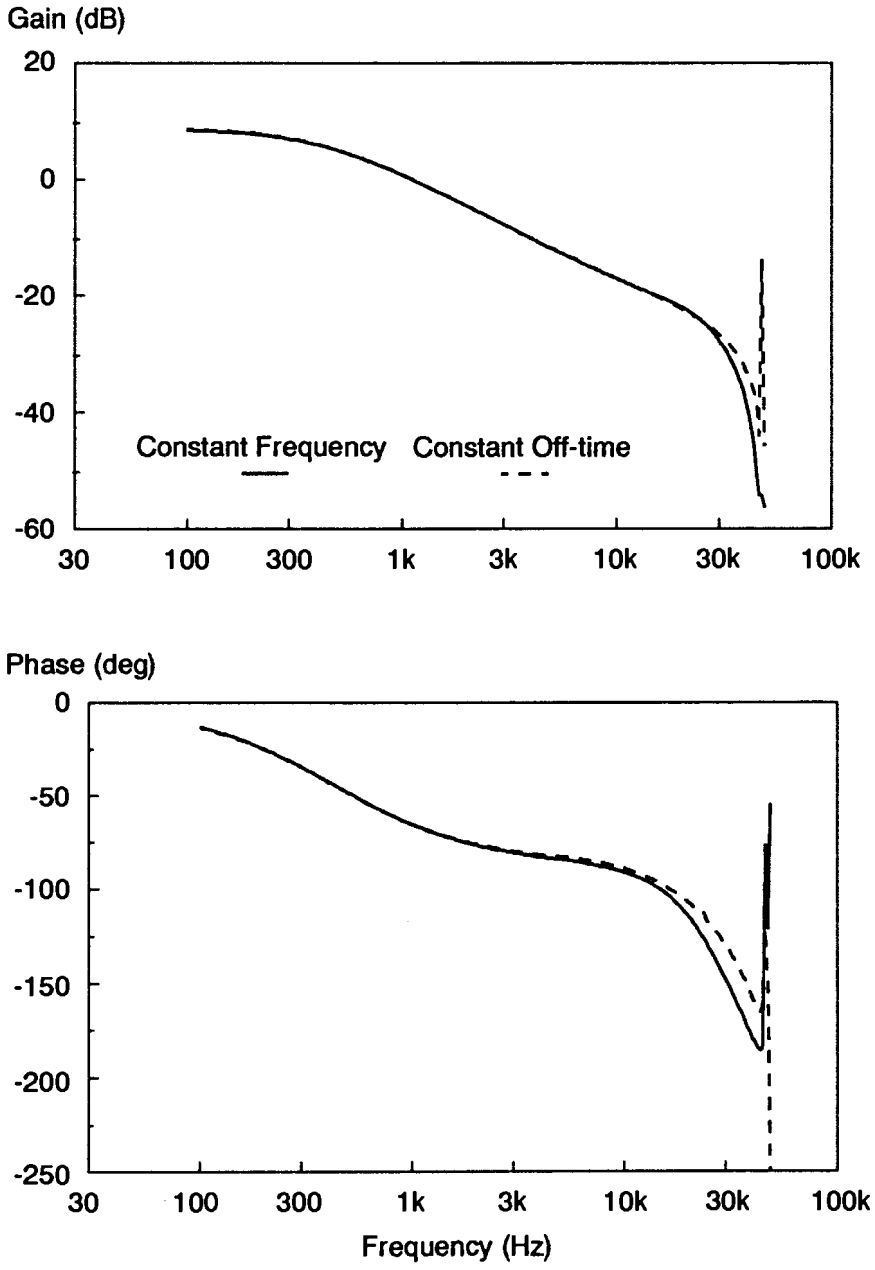


Figure 5.20. ***Control-to-Output Measurement for Constant-Frequency and Constant Off-Time, $D = 0.1$:*** *For very low duty cycles, these transfer functions are almost identical. The phase lead introduced by the modulator is small at low duty cycles, less than 10° at half the switching frequency. Like the constant-frequency control system, this transfer function has a pair of poles at half the switching frequency. These poles have a fixed Q of $2/\pi$, regardless of duty cycle.*

the plots of Fig. 5.22 was $D = 0.4$. In both of these figures, the measurements and predictions agree very well up to half the switching frequency. Comparison of the phase of these two figures clearly indicates how the modulator phase lead is increased with duty cycle. There is approximately thirty degrees phase difference between the two measurements at half the switching frequency.

The existence of phase lead in the constant off-time modulator is a phenomenon not previously discussed in the literature. Based upon the work in [36] for constant-frequency, naturally-sampled modulators, it is often assumed that naturally-sampled, variable-frequency schemes would be similar. The model of Fig. 4.5 for constant off-time control also predicts that the voltage-mode control system will have the same phase lead effect as the current-mode system. Again, this has not been remarked upon in the literature.

Measurements of current-mode and voltage-mode systems are presented in Fig. 5.23. Like the constant-frequency measurements of Fig. 5.7, the phase of the voltage-mode and current-mode systems are coincident at the power stage resonant frequency, and at half the switching frequency. Comparison of the phase of Fig. 5.23 and Fig. 5.7 with large external ramp shows clearly the phase lead of the constant off-time system for voltage-mode control.

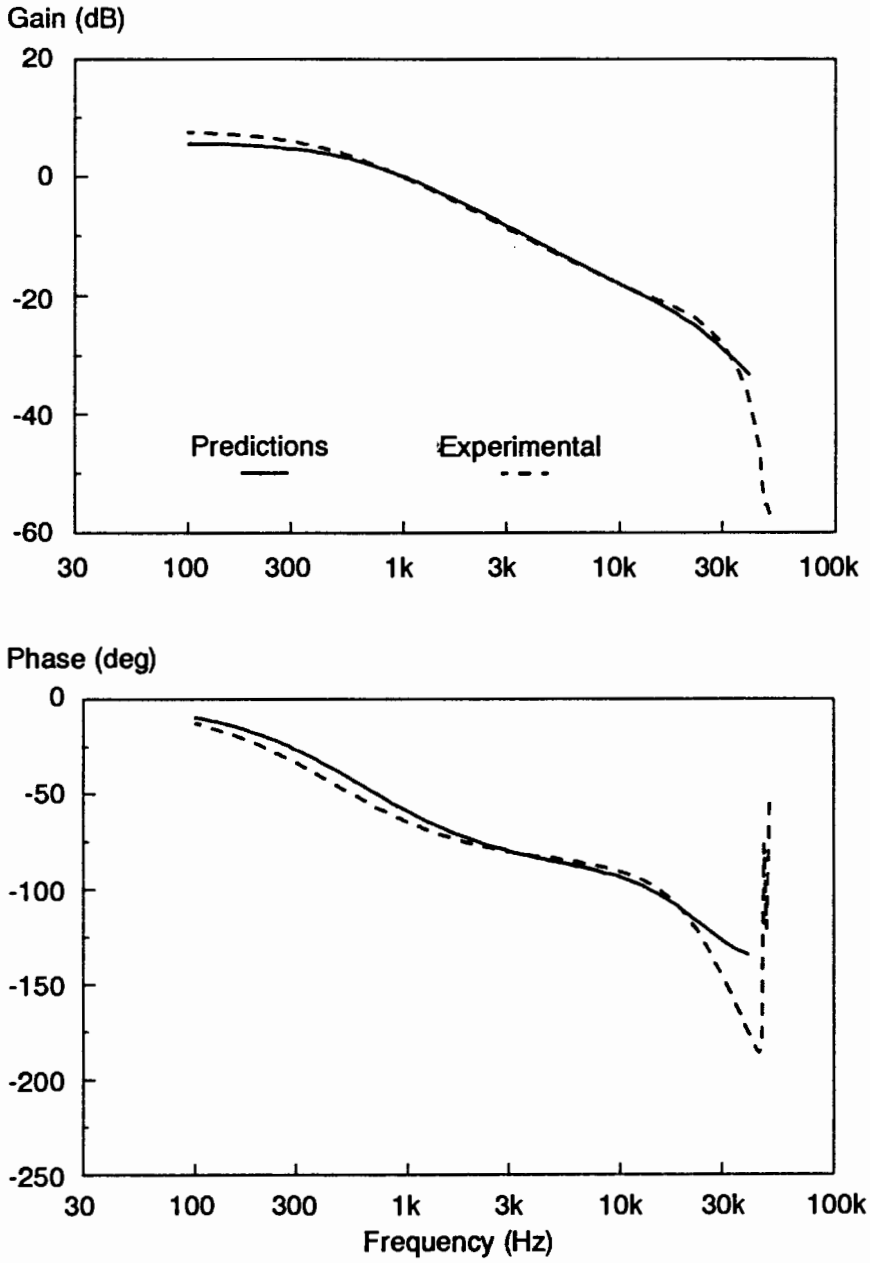


Figure 5.21. Control-to-Output Measurement and Theory for Constant Off-Time, D = 0.1: Measurement and theory agree very well for this transfer function up to 25 kHz, half the switching frequency.

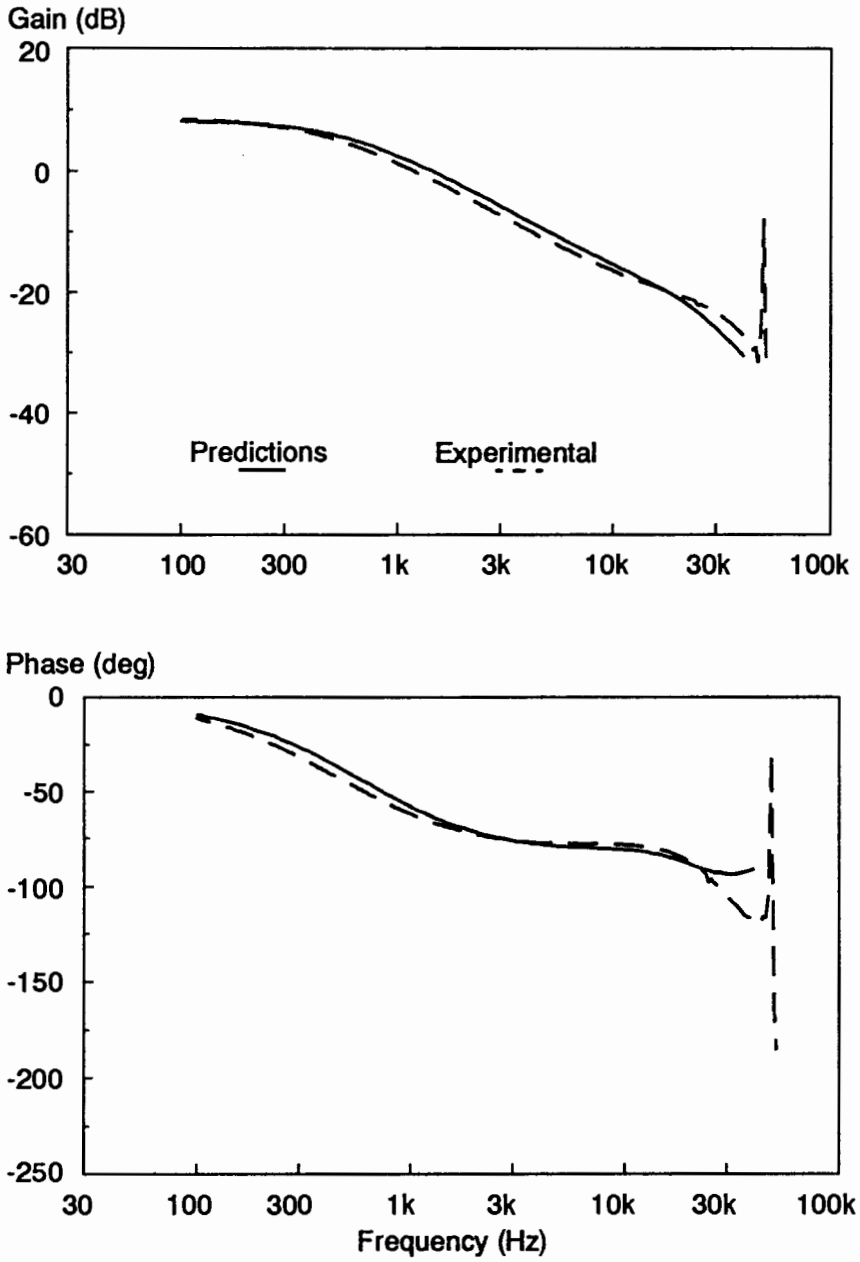


Figure 5.22. Control-to-Output Measurement and Theory for Constant Off-Time, D = 0.4: At higher duty cycles, the effect of the modulator phase lead F_c becomes significant. The double pole at half the switching frequency is still present in this transfer function.

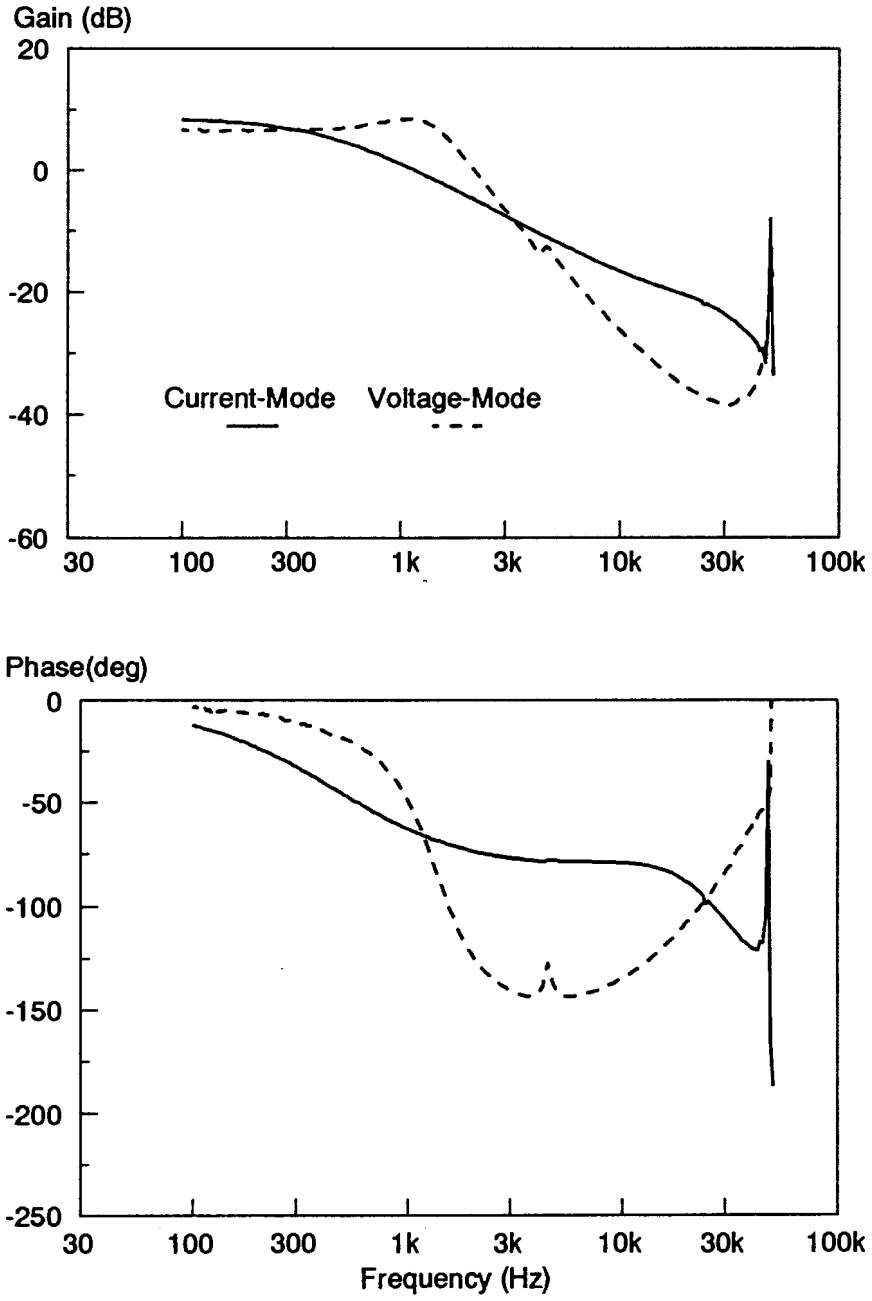


Figure 5.23. ***Control-to-Output Measurement for Voltage-Mode and Current-Mode Control:*** *The modulator phase characteristics also affect voltage mode control, obtained when the current sense resistor, R_i, is zero. The intersection of the phase of the current-mode system and the voltage-mode system at half the switching frequency is further experimental confirmation of the existence of the double pole at half the switching frequency in the current mode transfer function.*

5.4 Constant-Frequency Control in DCM

The models obtained in Chapter 4 for for DCM converters give several interesting predictions. The buck converter is especially interesting since it has a positive feedback term for k_r which can cause instability under the correct conditions. This effect has been noted previously in [42]. The control-to-output transfer function of the buck converter in DCM with constant-frequency control is easily obtained from the circuit diagram of Fig. 5.24.

This gain is given by

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m \frac{\hat{v}_o}{\hat{d}}}{1 - k_r F_m \frac{\hat{v}_o}{\hat{d}}} \tag{5.23}$$

The transfer function for the power stage, $\frac{\hat{v}_o}{\hat{d}}$, can be found from the PWM switch model for DCM operation to give [15]

$$\frac{\hat{v}_o}{\hat{d}} = H_d \frac{1 + \frac{s}{\omega_{z1}}}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \tag{5.24}$$

where

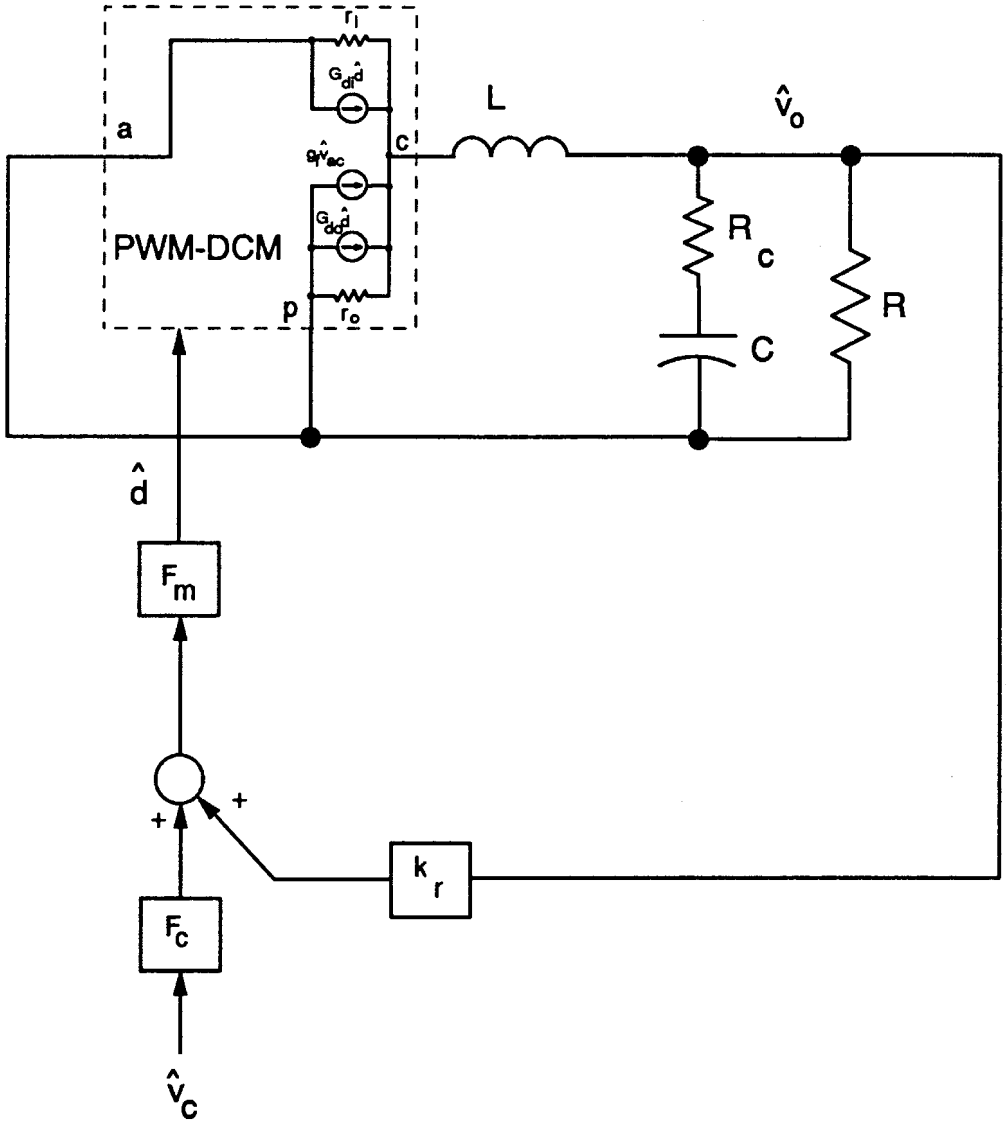


Figure 5.24. ***Circuit for Control-to-Output Derivation for the Buck Converter in DCM:*** *The power stage operating in DCM is replaced with the PWM switch model of Fig. 4.10, and the feedforward gain k_r is given in Table 4.7. Feedforward gain k_f does not appear since input perturbations are zero. Feedback of the inductor current does not explicitly appear in the small-signal model.*

$$H_d = \frac{2V_o}{D}\frac{1-M}{2-M} \tag{5.25}$$

$$\omega_{z1} = \frac{1}{CR_c} \tag{5.26}$$

$$\omega_{p1} = \frac{1}{CR}\frac{2-M}{1-M} \tag{5.27}$$

$$\omega_{p2} = 2F_s\left(\frac{M}{D}\right)^2 \tag{5.28}$$

Substituting for each of the gains in Eq. (5.23), and realizing that $\omega_{p1} << \omega_{z1}$ and $\omega_{p1} << \omega_{p2}$, the control-to-output is derived to give:

$$\frac{\hat{v}_o}{\hat{v}_c} = F_m H_c \frac{1+\frac{s}{\omega_{z1}}}{(1+\frac{s}{\omega_{p1}'})(1+\frac{s}{\omega_{p2}})} \tag{5.29}$$

where

$$H_c = \frac{2m_c V_o}{D}\frac{1-M}{2m_c-(2+mc)M} \tag{5.30}$$

$$\omega_{p1}' = \frac{1}{CR}\frac{2m_c-(2+m_c)M}{m_c(1-M)} \tag{5.31}$$

This transfer function shows the behavior of the constant-frequency buck converter with current-mode control in DCM. The instability mechanism is quite

different from that observed with CCM. The low-frequency pole of Eq. (5.29), ω_{p1}', is a function of the conversion ratio, M, of the converter. If no external ramp is used ($m_c = 1$), the pole moves to the origin at a conversion ratio of two-thirds, and into the right-half plane for higher conversion ratios. The observed unstable behavior of the converter is quite unlike the constant-frequency system where the approach of instability was manifested by high-Q double poles at half the switching frequency. These double poles cause 'jitter' to be observed in the waveforms as instability is approached. The DCM converter, on the other hand, starts to show very high low-frequency gain as the single pole approaches the origin. At the point of instability, the converter saturates as the pole moves into the right-half-plane. The instability can be mitigated by the addition of an external ramp, allowing higher conversion ratios. The use of the external ramp is recommended under all conditions for a buck converter with current-mode control.

The buck converter described in section 5.2 of this dissertation was run with the following parameters in discontinuous conduction mode:

$$R = 6.25\Omega \qquad V_g = 25V$$

The conversion ratio, and hence the output voltage of the DCM converter, was varied for the control-to-output measurements.

Fig. 5.25 shows predictions given by the transfer function of Eq. (5.29), and experimental measurements for the control-to-output transfer function with the current loop closed. From the gain curves for M=0.2 and M=0.64, the mi-

gration of the low-frequency pole towards the zero-frequency axis as the conversion ratio increases can clearly be seen. The low-frequency phase plots also confirm this pole movement. The measurements and theoretical data agree well for low values of M at all frequencies. For higher values of M, the measurements deviated from theory at higher frequencies.

It should be pointed out that the buck converter was very difficult to hold stable under conditions with M close to two-thirds. In addition to the low-frequency pole which made the dc gain of the system very high, parasitic ringing of device capacitance when the inductor current went to zero seemed to affect the measurements, even when these parasitics were minimized and snubbed. These effects may have caused the deviations at higher conversion ratios.

5.5 Conclusions

In this chapter, the application of the new small-signal model to a buck converter is described, with many important new conclusions about current-mode systems. The current-loop gain was shown to have an instability which is clearly explained by the small-signal model which shows a pair of RHP zeros at half the switching frequency. As the crossover frequency approached the theoretical maximum, the Nyquist frequency, the phase dropped to -180 degrees. The increase in gain of the current loop with conventional constant-frequency control occurs with increasing

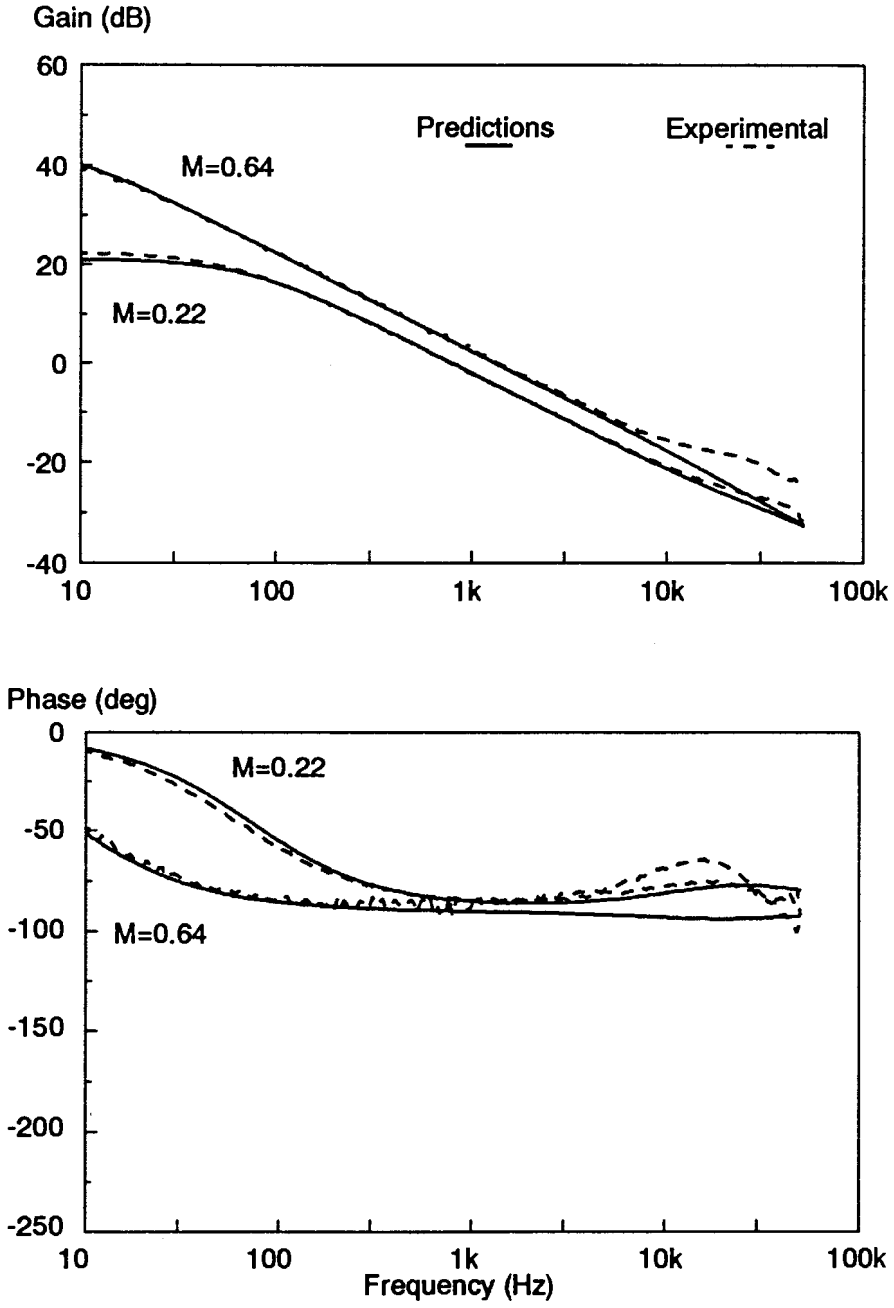


Figure 5.25. ***Control-to-Output Transfer Function for Buck Converter (DCM):*** *As the conversion ratio of the converter increases, the dominant pole of the system moves towards the zero axis. When the conversion ratio exceeds 0.67, this pole crosses into the right-half plane, and the system becomes unstable.*

duty cycle. The decreasing phase margin approaching this point clearly shows the cause of the onset of oscillations. The current-loop gain of constant on-time and off-time systems is of exactly the same form as the constant-frequency system, but the gain does not change with frequency, and the loop is always stable.

The RHP zeros in the current loop manifest themselves in the control-to-output transfer function as a pair of poles at half the switching frequency. For *all* converters with constant-frequency, current-mode control, the expression for these poles is given by

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}} \tag{5.32}$$

where

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)} \tag{5.33}$$

This very simple expression is easy to use for design of the appropriate external ramp of the system.

The presence of three poles in the control-to-output transfer function of two-state converters explains why there was so much confusion in the past about different average models. Researchers argued the merits of two-pole systems versus one-pole systems, when in reality a *three*-pole model is needed for accurate predictions. The additional pole of the system does not complicate the design of the

converter or the use of the new model compared to previous models. Instead, it clearly explains for the first time the true nature of the phenomena of current-loop instability.

The presence of the pair of complex poles also showed clearly how the current-mode system can become unstable at duty cycles considerably less than 0.5, when output feedback compensation is added. The expression for the complex poles shows how to avoid this situation.

The audio susceptibility of the buck converter could be nulled with the appropriate value of external ramp, confirming observations in earlier works. Few of the previous average models were capable of predicting this result. Feedforward terms from the input voltage are required in the model, and although these exist in some average approaches, the values of these terms were found to be different in the new model.

The new model was also applied to DCM operation, showing how the buck converter could have a RHP pole with higher conversion ratios. It was shown how an external ramp could be used to stabilize this system.

6. Conclusions

A new small-signal model has been derived for current-mode control in continuous-conduction mode and discontinuous-conduction mode. The new model provides improved accuracy at low frequencies and at high frequencies compared to existing average models. It retains all of the advantages of simplicity and ease-of use of popular continuous-time models with polynomial pole-zero representations.

Sampled-data modeling was used for exact analysis of the current-mode cell which is basic to all PWM converters with current-mode control. The usual complexities involved with sampled-data modeling were avoided by applying this analysis to just the first-order system which requires the accurate high-frequency modeling. The result obtained from the sampled-data analysis was then further simplified by an approximate polynomial transfer function. An invariant second-order expression provided remarkable accuracy at frequencies from dc to

half the switching frequency. The analysis was completed by modeling the affects of changing voltages across the current-mode cell with two feedforward gains.

The second-order approximation to the one-state, sampled-data results provides several new observations for the current-mode converter. Firstly, the current-loop gain of the converter was shown to have a pair of RHP zeros at half the switching frequency which shows the possibility of instability in this loop. The phase margin of the current loop goes to zero as the crossover frequency goes to half the switching frequency. This is completely consistent with Nyquist sampling theory.

The low phase margin that exists in the current loop under some conditions produces a pair of complex poles in the control-to-output transfer function at half the switching frequency. The damping of these poles is predicted by a very simple expression which can then be used to select the correct external ramp for the system.

The three-pole transfer function for two-state converters clearly explains why previous average models, which had at most two poles, could not be satisfactorily used for this system. Much debate in the past has revolved around the position of the second pole of the system, or whether it was even needed at all in the model since it was assumed to be at very high frequency. It is now clear that *two* high-frequency poles are required for accurate modeling, and the system can only be

approximated with one high-frequency pole if an inordinately large external ramp is added to the current-mode modulator.

The new model was extended to variable-frequency control schemes which do not generally have the problem of an unstable current loop. It was shown that even these systems have the same RHP zeros in the current loop, but they remain stable since the current-loop gain does not change with operating conditions. An interesting observation of modulator phase-lead was also made for the variable-frequency schemes used in this dissertation. This effect has not been discussed in the literature before with respect to power electronics.

Other effects which have been seen in the past have also been explained. The observation that the audio susceptibility of a buck converter can be completely nulled with an appropriate value of external ramp was confirmed by the new model. This can only happen with a model which has feedforward terms from the input voltage. The feedforward terms are an integral part of the new model, but not of all previous averaging models.

The DCM model for current-mode control is very simple. Assuming that the power stage model is accurate, only feedforward terms are required in the current-mode model. The current loop does not even appear explicitly in the small-signal model. No sampled-data modeling was required for the current-mode feedback in DCM. Application of the new model to the buck converter in DCM showed how the converter could be unstable at high conversion ratios.

The new small-signal model is very easy to use for converter design and analysis. To facilitate its use, appendices have been provided to summarize important results and give equivalent circuit models for computer simulation. Since the new model retains the original power stage model and the duty cycle control parameter, it can be applied to any converter with either voltage-mode or current-mode control.

Appendix A - Summary of Results

A.1 Introduction

The detailed analysis of Chapters 3 and 4 of this dissertation resulted in the derivation of new small-signal models for current-mode control. The important elements of the new models are summarized for convenience in this appendix for both continuous- and discontinuous-conduction modes.

A.2 Continuous-Mode Model

The new circuit model for current-mode control is shown in Fig. A.1 for continuous-conduction mode operation. The power stage model is provided by

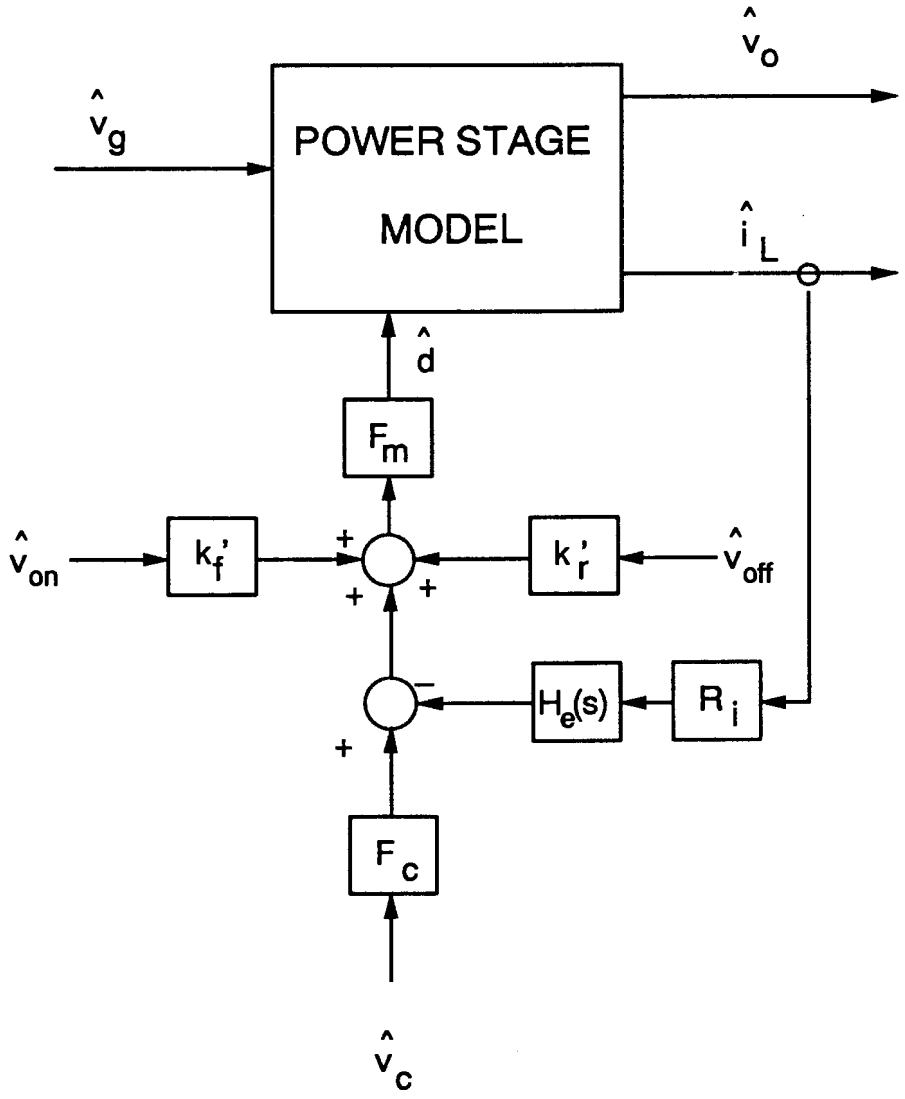


Figure A.1. ***Small-Signal Model for Continuous-Conduction Mode:*** *The model shown in this figure is invariant for all PWM converters, and can be used for current-mode or voltage-mode control ($R_i = 0$). All transfer functions, including the current-loop gain, can be generated with this model. Parameter values for the model are given in Table A.1 for the different modulation strategies.*

the PWM switch model, described in Chapter 2, and derived in [15]. The important terms of the model of Fig. A.1 are the modulator gain, F_m, the sampling gain, $H_e(s)$, and the gains, k_f' and k_r', from the on-time and off-time inductor voltages.

This form of the new current-mode model is the most convenient representation since the gains of the model are invariant for all converters for a given modulation scheme. An alternative form of the model, given in Fig. 4.6, uses gain terms from the input and output voltages of the specific power stage, resulting in an equivalent model which changes for each power stage topology.

Table A.1 summarizes the parameter values for the model of Fig. A.1, for the four different implementations of current-mode control discussed in this work. For most readers of this dissertation, the control scheme used is constant-frequency with a clock initiating the on-time, and only the parameters in the first column of the table are needed. Also, for the constant-frequency control schemes, the modulator gain block, F_c, is not needed since it has a value of one.

The model of Fig. A.1 is quite universal. It can be applied to any PWM converter which can be modeled with the PWM switch, and can be used for either current-mode or voltage-mode control. With voltage-mode control, the feedback gain term $R_i = 0$, and the current feedback loop is open. Notice that the other parameters, k_f' and k_r', are also zero with voltage-mode control, leaving just the modulator gain, F_m and F_c, in the voltage-mode model.

TABLE A.1
Parameter Values for Continuous-Conduction-Mode

	Constant Frequency Trailing Edge	Constant Frequency Leading Edge	Constant Off-Time	Constant On-Time
k_f'	$-\frac{DT_s R_i}{L}\left[1-\frac{D}{2}\right]$	$-\frac{D^2 T_s R_i}{2L}$	$-\frac{DT_s R_i}{L}$	$-\frac{DT_s R_i}{2L}$
k_r'	$\frac{D'^2 T_s R_i}{2L}$	$\frac{D'T_s R_i}{L}\left[1-\frac{D'}{2}\right]$	$\frac{D'T_s R_i}{2L}$	$\frac{D'T_s R_i}{L}$
F_m	$\frac{1}{(S_n+S_e)T_s}$	$\frac{1}{(S_f+S_e)T_s}$	$\frac{D'}{S_n T_s}$	$\frac{D}{S_f T_s}$
F_c	1	1	$e^{sDT_s/2}$	$e^{sD'T_s/2}$
$H_e(s)$	$1+\frac{s}{\omega_n Q_z}+\frac{s^2}{\omega_n^2}$		$Q_z=\frac{-2}{\pi}$	$\omega_n=\frac{\pi}{T_s}$

A.3 Discontinuous-Mode Model

Fig. A.2 shows the small-signal model for discontinuous-conduction mode. This model is much simpler than that for the continuous conduction mode, consisting of the power stage model, modulator gain, and a feedforward term, k_f', from the

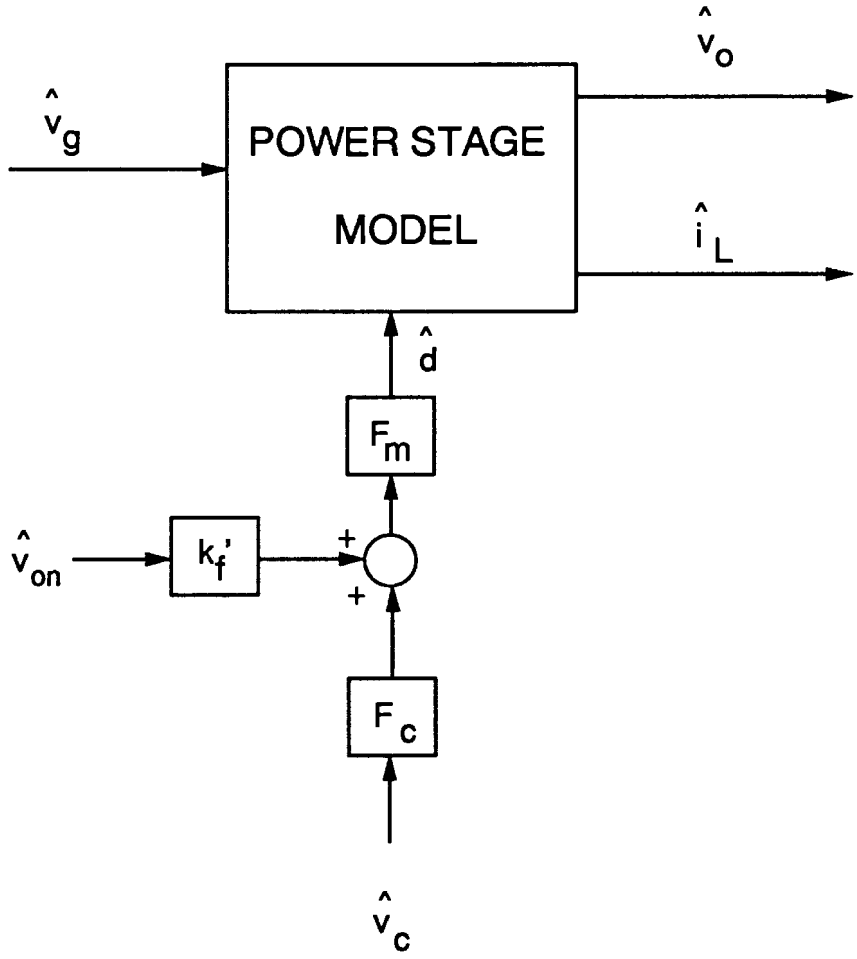


Figure A.2. ***Small-Signal Model for Discontinuous-Conduction Mode:*** *This invariant model is used for all converters in DCM. It is valid for both current-mode and voltage-mode control. Notice that the current feedback does not explicitly appear in the model. Parameter values for the model are given in Table A.2.*

on-time voltage across the inductor. The current feedback loop does not explicitly appear in this model.

Table A.2 gives the parameter values associated with the model of Fig. A.2. Only two control schemes are modeled since constant on-time and constant-frequency with a clock initiating the off-time cannot be used with current-mode control in DCM. Both of these schemes use feedback of the inductor current at the end of the off-time of the converter. In DCM, of course, the current is zero at this time.

TABLE A.2
Parameter Values for Discontinuous-Conduction-Mode

	Constant Frequency	Constant Off-Time
F_m	$\frac{1}{(S_n + S_e)T_s}$	$\frac{D'}{S_n T_s}$
F_c	1	$e^{sDT_s/2}$
k_f'	$-\frac{DT_s R_i}{L}$	

Appendix B - PSPICE Modeling

B.1 Introduction

The derivations used in Chapters 3 and 4 of this dissertation are fairly involved. However, the resulting small-signal model, and the approximations to the sampling function, are very simple. This leads to convenient representations of the current-mode control model, summarized in Appendix A, which can very easily be implemented in PSpice [43], or any other circuit simulation program.

This appendix provides the listings of PSpice models for a generic controller for *any* PWM converter which can be modeled with the PWM switch, using constant-frequency control with a clock initiating the on-time. The controller can be used for either current-mode, or voltage-mode control, and listings are provided for both continuous-conduction mode and discontinuous-conduction mode.

For many readers, this appendix is the most important part of this dissertation. It provides a simple model which can be readily applied to a converter, without detailed understanding of the derivations of this work.

B.2 Universal PWM Control Module

Fig. B.1 shows the functional diagram of the controller for either voltage-mode, or current-mode control. The subcircuit of the controller, called *PWMCCM*, contains the PWM switch model, modulator gain, F_m, current feedback and sampling gains, R_i and $H_e(s)$, and feedforward terms, k_f' and k_r'.

Five external connections must be made to the controller. These are the active terminal connection, the passive terminal connection, the common terminal, the control voltage input, and the voltage from the far side of the power stage inductor from the common terminal. This final connection is required to provide the inputs to the gain terms, k_f' and k_r'. Notice that the on-time voltage is now denoted by $\hat{v}_{ac'}$, where c' is the external connection to the far side of the inductor of the power stage. The off-time voltage is given by $\hat{v}_{c'p}$. The connection c' is shown more clearly in Fig. B.3.

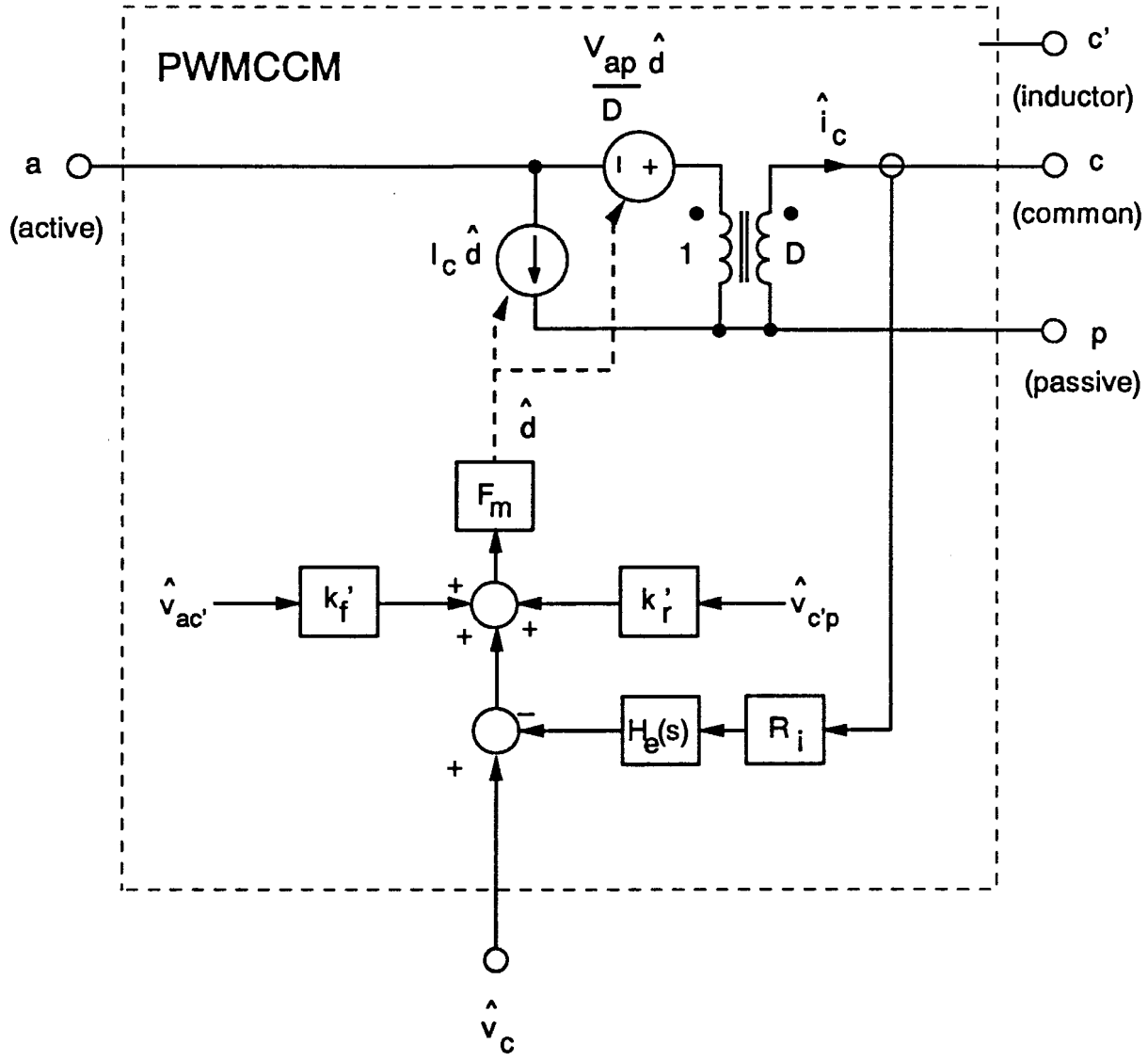


Figure B.1. Small-Signal Controller Model for Voltage-Mode and Current-Mode Control in CCM: The new controller model, referred to as PWMCCM, incorporates the feedback control and power stage PWM switch into one convenient subcircuit. Five connections must be defined for the subcircuit.

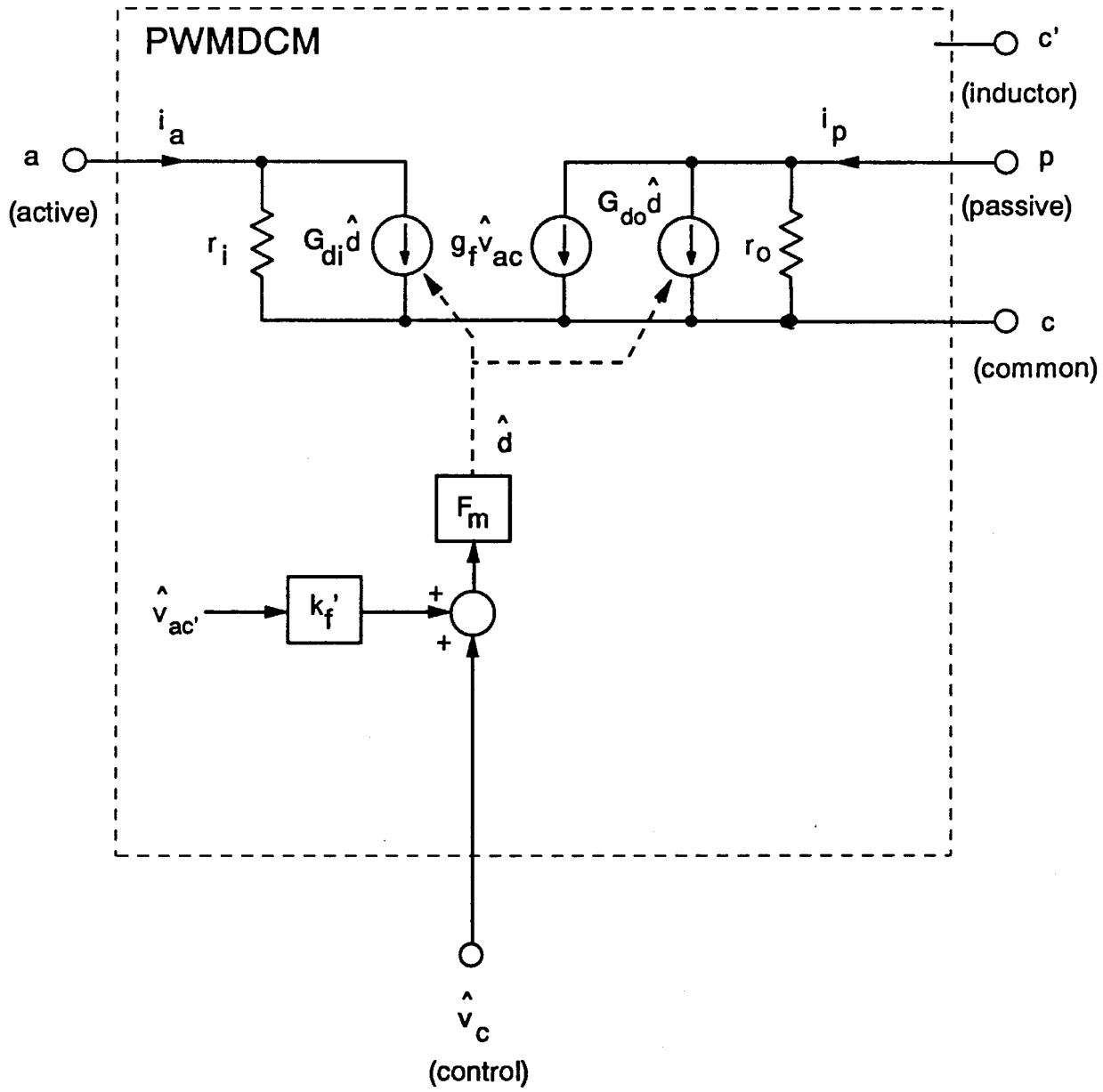


Figure B.2. ***Small-Signal Controller Model for Voltage-Mode and Current-Mode Control in DCM:*** *The controller model, referred to as PWMDCM, incorporates the feedback control and power stage PWM switch model for discontinuous conduction mode into one convenient subcircuit.*

Fig. B.2 shows the controller module for discontinuous conduction mode. The power stage switch model for DCM is used, and the controller only needs the modulator gain, F_m, and the feedforward gain, k_f'. Notice that the notation on the PWM switch model for DCM operation is different from that originally used in [15]. The conductances of the model have been changed to resistances, and the names of the sources are changed to be consistent with units and the PSpice models given below. The model behaves exactly the same as the original PWM switch model for DCM.

Fig. B.3 shows how the controller subcircuit, *PWMCCM*, is connected to the four most common types of converter. (For discontinuous conduction mode, the circuit diagrams remain the same, but the *PWMDCM* model is used.) The universal form of the model requires that conventions must be followed in its use. The current sensing implemented is referred to the inductor current flowing *out* of the common terminal of the switch. For the boost converter, the standard way to draw the circuit is with the current flowing *into* the common terminal. The circuit conforms to the required conventions if the value of R_i is negative. This also affects the polarity of k_f' and k_r' of the boost model.

The Cuk converter is a circuit where the *sum* of two inductor currents is controlled. In this case, the parallel combination of the two inductors of the circuit is used in calculating k_f' and k_r', and the modulator gain, F_m. Also, the position of one of the inductors must be moved, as shown in Fig. B.3d, to provide the correct connection to the *PWMCCM* subcircuit.

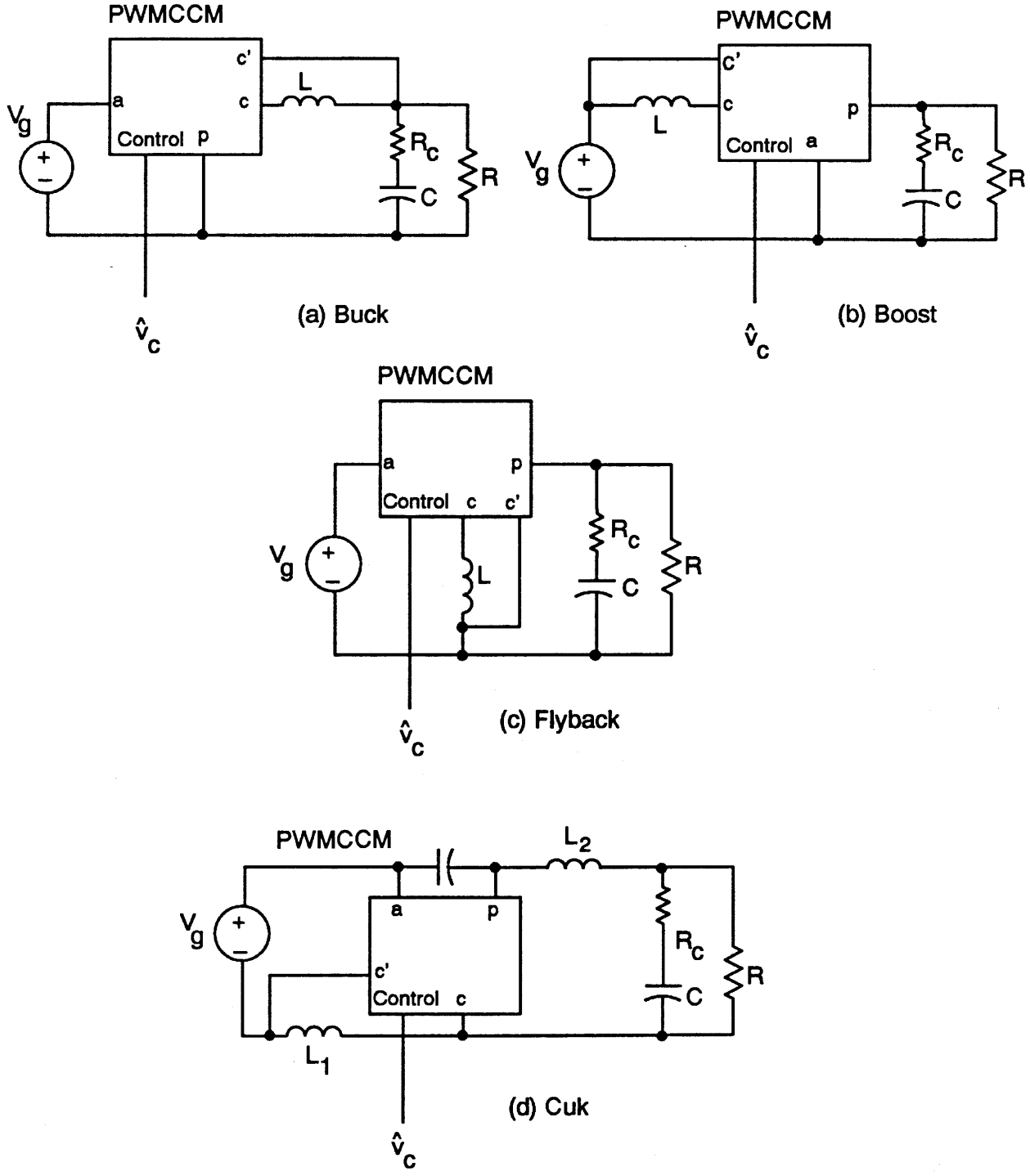


Figure B.3. ***Small-Signal Controller Placed in Different Converters:*** *Connections of the controller of Fig. B.1 in four types of PWM circuits are shown. Care must be taken with polarities of current sensing for the boost converter, and with the correct value of equivalent inductance for the Cuk converter.*

```
* Buck Converter Model. R. Ridley   *
*************************************
    Vin    1   0     AC    0
    Rl     2   4     0.02
    L      4   5     37.5uH
    Rc     5   6     0.02
    C      6   0     400uF
    R      5   0     1
    Vc    11   0     AC    1
    X1     1   0  2   5   11   PWMCCM
 .AC     DEC    25    10HZ 50KHZ
 .PROBE

* PWMCCM:      Active Passive Common Inductor Control
.SUBCKT PWMCCM  1        2        3       4        5
 * Switch model: E2=Vap/D G1=Ic Fxf=D Exf=D
     E2    7   1 17   0      24.44
     G1    1   2 17   0       5.0
     Fxf   7   2     Vxf      0.45
     Exf   9   2   7   2      0.45
     Vxf   9   3     0
     Rvc   5   0     1G
 * He(s) Circuit values:  L1=C1=C2 = Ts/Pi
     Hi   10   0     Vxf    1
     C1   10  12     6.37uF
     L1   12  13     6.37uH
     C2   13  14     6.37uF
     Re   14  15     -1.57
     E1   15   0 12   0   -1E6
     R2   12   0     1G
 * Summing Gains:                              0     Kf'     Kr'    Ri  1
     Ed   16   0  Poly(4) 1,4 4,2 15,0 5,0 0 -0.0614 0.0266 0.33 1
     Rd   16   0  1G
 * Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
     EFm 17   0 16   0    0.939
     RFm 17   0     1G
.ENDS
.END
```

Figure B.4. PSpice Listing for the CCM Buck Converter Example of Chapter 5: This file was used with the parameters shown to generate the control-to-output curve of Fig. 5.7 with no external ramp ($m_c = 1$). The listing here gives the connections of the buck converter to the controller.

The model listings of four converters are provided in this appendix. In each of the models, the parasitic resistances of the inductors are included to provide a more realistic model. It is a very simple task to create the files for other converters which use the common small-signal controller model.

The listing is given in Fig. B.4 for the buck converter example used in Chapter 5. The specific set-up and parameter values shown are for generating the control-to-output curve of Fig. 5.7 with no external ramp ($m_c = 1$). Fig. B.5 repeats the buck converter listing to show which values must be entered into the model by the user when modeling a different circuit.

The listing given in Fig. B.6 is for the buck converter example used in Chapter 5 in discontinuous mode. The specific set-up and parameter values shown are for generating the control-to-output curve of Fig. 5.25 with a conversion ratio of $M = 0.2$). Fig. B.7 repeats the DCM buck converter listing to show which values must be entered into the model by the user when modeling a different circuit.

Figs. B.8-B.10 give the listings for boost, flyback, and Cuk converters. Each of these different power stages uses the same *PWMCCM* subcircuit with the appropriate values. The discontinuous-mode model is obtained by using the subcircuit *PWMDCM*.

```
* Buck Converter Model. R. Ridley   *
*************************************
    Vin    1   0     AC    0
    Rl     2   4     ##
    L      4   5     ##
    Rc     5   6     ##
    C      6   0     ##
    R      5   0     ##
    Vc    11   0     AC    1
    X1     1   0  2   5   11   PWMCCM
 .AC     DEC    25    10HZ 50KHZ
 .PROBE

* PWMCCM:      Active Passive Common Inductor Control
.SUBCKT PWMCCM  1        2        3       4        5
 * Switch model: E2=Vap/D G1=Ic Fxf=D Exf=D
     E2    7   1 17   0      ##
     G1    1   2 17   0      ##
     Fxf   7   2     Vxf     ##
     Exf   9   2   7   2     ##
     Vxf   9   3     0
     Rvc   5   0     1G
 * He(s) Circuit values:  L1=C1=C2 = Ts/Pi
     Hi   10   0     Vxf    1
     C1   10  12     ##
     L1   12  13     ##
     C2   13  14     ##
     Re   14  15     -1.57
     E1   15   0 12   0   -1E6
     R2   12   0     1G
 * Summing Gains:                              0     Kf'     Kr'    Ri   1
     Ed   16   0   Poly(4) 1,4 4,2 15,0 5,0 0     ##      ##     ##   1
     Rd   16   0   1G
 * Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
     EFm 17   0 16   0    ##
     RFm 17   0     1G
.ENDS
.END
```

Figure B.5. PSpice Listing for a Buck Converter in CCM: *This file can be used for any buck converter to be modeled. Parameters marked with ## must be supplied by the user.*

```
* Buck Converter Model. R. Ridley   *
*************************************
    Vin    1   0     AC    0
    Rl     2   4     0.05
    L      4   5     37.5uH
    Rc     5   6     0.02
    C      6   0     400uF
    R      5   0     6.25
    Vc    11   0     AC    1
    X1     1   0  2   5   11   PWMDCM
 .AC     DEC    25    10HZ 50KHZ
 .PROBE


* PWMDCM:      Active Passive Common Inductor Control
.SUBCKT PWMDCM    1       2       3       4       5
 * Switch: ri=Vac/Ia Gdi=2Ia/D gf=2Ip/Vac Gdo=2Ip/D ro=Vcp/Ip
     ri    1   3     125
     Gdi   1   3 17   0   2
     gf    2   3   1   3     0.064
     Gdo   2   3 17   0   8
     ro    2   3     7.81
     Rvc   5   0     1G

 * Summing Gains:                  0     Kf'    1
     Ed   16   0   Poly(2) 1,4 5,0 0 -0.0282   1
     Rd   16   0   1G
 * Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
     EFm 17   0 16   0    0.284
     RFm 17   0     1G
.ENDS
.END
```

Figure B.6. PSpice Listing for the DCM Buck Converter Example of Chapter 5: This file was used with the parameters shown to generate the control-to-output curve of Fig. 5.25 with a conversion ratio of $M = 0.2$.

```
* Buck Converter Model. R. Ridley   *
*************************************
    Vin    1   0     AC    0
    Rl     2   4     ##
    L      4   5     ##
    Rc     5   6     ##
    C      6   0     ##
    R      5   0     ##
    Vc    11   0     AC    1
    X1     1   0  2   5   11   PWMDCM
 .AC     DEC    25    10HZ 50KHZ
 .PROBE


* PWMDCM:      Active Passive Common Inductor Control
.SUBCKT PWMDCM    1       2        3        4        5
 * Switch: ri=Vac/Ia Gdi=2Ia/D gf=2Ip/Vac Gdo=2Ip/D ro=Vcp/Ip
     ri    1   3     ##
     Gdi   1   3 17   0   ##
     gf    2   3   1   3   ##
     Gdo   2   3 17   0   ##
     ro    2   3     ##
     Rvc   5   0     1G

 * Summing Gains:                    0     Kf'    1
     Ed   16   0   Poly(2) 1,4 5,0   0     ##     1
     Rd   16   0   1G
 * Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
     EFm 17   0 16   0    ##
     RFm 17   0     1G
.ENDS
.END
```

Figure B.7. PSpice Listing for a DCM Buck Converter: This file can be used for any buck converter in DCM to be modeled. Parameters marked with ## must be supplied by the user.

```
* Boost Converter Model. R. Ridley   *
*************************************
    Vin     1     0     AC   0
    Rl      1     2     ##
    L       2     4     ##
    Rc      5     6     ##
    C       6     0     ##
    R       5     0     ##
    Vc    11   0     AC    1
    X1      0     5     4     1    11    PWMCCM

 .AC     DEC    25    10HZ 50KHZ
 .PROBE

* PWMCCM:      Active Passive Common Inductor Control
.SUBCKT PWMCCM  1        2        3       4        5
 * Switch model: E2=Vap/D G1=Ic Fxf=D Exf=D
     E2    7   1 17   0      ##
     G1    1   2 17   0      ##
     Fxf   7   2     Vxf     ##
     Exf   9   2   7   2      ##
     Vxf   9   3     0
     Rvc   5   0     1G
 * He(s) Circuit values:  L1=C1=C2 = Ts/Pi
     Hi   10   0     Vxf    1
     C1   10  12     ##
     L1   12  13     ##
     C2   13  14     ##
     Re   14  15     -1.57
     E1   15   0 12   0   -1E6
     R2   12   0     1G
 * Summing Gains:                              0     Kf'     Kr'    Ri   1
     Ed   16   0   Poly(4) 1,4 4,2 15,0 5,0 0     ##      ##     ##   1
     Rd   16   0   1G
 * Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
     EFm 17   0 16   0    ##
     RFm 17   0     1G
.ENDS
.END
```

Figure B.8. PSpice Listing for a Boost Converter in CCM: *This can be used to generate the transfer functions of a boost converter. Parameters marked with ## must be filled in for the circuit being modeled. Care must be taken with the polarity of the current sensing. The conventional boost circuit polarities shown, for example, in Fig. B.3 should have a negative value for R_i, since the defined inductor current flows into the common terminal.*

```
* Flyback Converter Model. R. Ridley   *
*************************************
    Vin     1     0     AC    0
    Rl      3     2     ##
    L       2     0     ##
    Rc      5     6     ##
    C       6     0     ##
    R       5     0     ##
    Vc    11   0     AC    1
    X1      1     5     3     0    11    PWMCCM

 .AC    DEC   25   10HZ 50KHZ
 .PROBE

* PWMCCM:     Active Passive Common Inductor Control
.SUBCKT PWMCCM  1       2       3       4       5
 * Switch model: E2=Vap/D G1=Ic Fxf=D Exf=D
     E2    7   1 17   0      ##
     G1    1   2 17   0      ##
     Fxf   7   2     Vxf     ##
     Exf   9   2   7   2      ##
     Vxf   9   3     0
     Rvc   5   0     1G
 * He(s) Circuit values:  L1=C1=C2 = Ts/Pi
     Hi   10   0     Vxf    1
     C1   10 12      ##
     L1   12 13      ##
     C2   13 14      ##
     Re   14 15      -1.57
     E1   15   0 12   0   -1E6
     R2   12   0     1G
 * Summing Gains:                                0     Kf'     Kr'    Ri   1
     Ed   16   0   Poly(4) 1,4 4,2 15,0 5,0 0     ##      ##     ##   1
     Rd   16   0   1G
 * Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
     EFm 17   0 16   0    ##
     RFm 17   0     1G
.ENDS
.END
```

Figure B.9. ***PSpice Listing for a Flyback Converter in CCM:*** *This data file can be used to generate the transfer functions of a flyback converter. Parameters marked with ## must be filled in for the circuit being modeled. The output of the flyback converter is negative, and this must be taken into consideration when designing the feedback circuit model.*

```
* Cuk Converter Model. R. Ridley    *
*************************************
    Vin    2   1     AC    0
    Rl1    1   3     ##
    L1     3   0     ##
    Cc     2   4     ##
    Rl2    4   7     ##
    L2     7   5     ##
    R      5   0     ##
    Rc     5   6     ##
    C      6   0     ##
    Vc    11   0     AC    1
    X1     2   4   0   1 11    PWMCCM

 .AC    DEC    25    10HZ 50KHZ
 .PROBE

* PWMCCM:      Active Passive Common Inductor Control
.SUBCKT PWMCCM  1        2        3       4        5
 * Switch model: E2=Vap/D G1=Ic Fxf=D Exf=D
     E2    7   1 17   0      ##
     G1    1   2 17   0      ##
     Fxf   7   2     Vxf     ##
     Exf   9   2   7   2      ##
     Vxf   9   3     0
     Rvc   5   0     1G
 * He(s) Circuit values:  L1=C1=C2 = Ts/Pi
     Hi   10   0     Vxf    1
     C1   10  12     ##
     L1   12  13     ##
     C2   13  14     ##
     Re   14  15     -1.57
     E1   15   0  12   0   -1E6
     R2   12   0     1G
 * Summing Gains:                                0     Kf'     Kr'    Ri   1
     Ed   16   0   Poly(4) 1,4 4,2 15,0 5,0 0     ##      ##     ##   1
     Rd   16   0   1G
 * Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
     EFm 17   0 16   0    ##
     RFm 17   0     1G
.ENDS
.END
```

Figure B.10. ***PSpice Listing for a Cuk Converter in CCM:*** *This data file can be used to generate the transfer functions of a Cuk converter. Parameters marked with ## must be filled in for the circuit being modeled. The output of the Cuk converter is negative, and this must be taken into consideration when designing the feedback circuit model. Also, the common current is the sum of the inductor currents; the parallel combination of inductances must be used in calculating* F_m, k_f' *and* k_r'.

Appendix C - Definition of Symbols

This appendix provides a reference for the common symbols used in this dissertation. Upper-case variables refer to steady-state or dc conditions, lower case denotes the continuous variable, and lower case with a caret is the small-signal perturbation around steady-state.

α	Discrete-time pole of current cell
d	Duty cycle
d'	Complement of duty cycle $1 - d$
$\Delta(s)$	Denominator of power stage transfer functions
f_c	Crossover frequency
F_c	Phase of duty cycle modulator
$F_h(s)$	High-frequency double pole with closed current loop
$F_i(s)$	Duty-cycle-to-inductor-current gain
F_m	Duty cycle modulator gain
$F_p(s)$	Average dynamics with closed current loop
F_s	Switching frequency
g_f	Forward conductance of DCM model
G_{di}	Control input source of DCM model

G_{do}	Control output source of DCM model
H_d	DC gain of buck power stage in DCM
$H_e(s)$	Equivalent sampling-gain block in current feedback
i_a	Current into the active terminal
i_p	Current into the passive terminal
i_c	Current out of the common terminal
i_L	Inductor current, same as i_c
k_f	Feedforward gain from input voltage to duty cycle
k_f'	Feedforward gain from on-time voltage to duty cycle
k_r	Feedforward gain from output voltage to duty cycle
k_r'	Feedforward gain from off-time voltage to duty cycle
m_c	External ramp parameter
P_w	Pulse width
Q_p	Q of double poles at half switching frequency
Q_{ps}	Q of poles of power stage filter
Q_z	Q of zeros of approximate sampling gain
r_i	Input resistance of DCM model
R_i	Current-sensing gain
r_o	Output resistance of DCM model
S_e	External ramp slope
S_f	Magnitude of off-time slope of current-sense signal
S_n	Magnitude of on-time slope of current-sense signal
T_f	Off-time of power switch
$T_i(s)$	Current loop gain
$T_i^{ave}(s)$	Current loop gain without sampling model
T_n	On-time of power switch
T_s	Switching period
ω_n	Half switching frequency in radians/sec
ω_o	Power stage filter resonant frequency in radians/sec
ω_p	Dominant pole with closed current loop
ω_{p1}	First pole of open-loop DCM converter

ω_{p2}	Second pole of open-loop DCM converter
v_{ac}	Voltage from active (+) to common terminal (-)
$v_{ac'}$	Voltage from active (+) to inductor (-)
v_{ap}	Voltage from active (+) to passive terminal (-)
v_c	Control voltage
v_{cp}	Voltage from common (+) to passive terminal (-)
$v_{c'p}$	Voltage from inductor (+) to passive (-).
v_g	Converter input voltage
v_o	Converter output voltage
v_{off}	Voltage across inductor when diode is on
v_{on}	Voltage across inductor when switch is on
$Z_o(s)$	Output impedance

References

1. L.E. Gallaher, "*Current Regulator with AC and DC Feedback,*" U.S. Patent 3,350,628, 1967.

2. A. Capel, G. Ferrante, D. O'Sullivan, A. Weinberg, "*Application of the Injected Current Model for the Dynamic Analysis of Switching Regulators with the New Concept of LC 3 Modulator,*" IEEE Power Electronics Specialists Conference, 1978 Record, pp.135-147.

3. F.C. Schwarz, "*Analog Signal to Discrete Time Interval Converter (ASDTIC),*" U.S. Patent 3,659,184, 1972.

4. A.D. Schoenfeld, Y. Yu, "*ASDTIC Control and Standardized Interface Circuits Applied to Buck, Parallel and Buck-Boost DC-to-DC Power Converters,*" NASA Report NASA CR-121106, Prepared by TRW Systems, February, 1973.

5. R.B. Ridley, B.H.Cho and F.C.Y. Lee, "*Analysis and Interpretation of Loop Gains of Multi-Loop-Controlled Switching Regulators,*" IEEE Transactions on Power Electronics, Vol. 3, No. 4, pp. 489-498, October 1988.

6. R.B. Ridley, "*Small-Signal Analysis of Parallel Power Converters,*" MS Thesis, Virginia Polytechnic Institute and State University, March 1986.

7. C.W. Deisch, "*Switching Control Method Changes Power Converter into a Current Source*" IEEE Power Electronics Specialists Conference, 1978 Record, pp.300-306.

8. P.F. Panter, "*Modulation, Noise, and Spectral Analysis, Applied to Information Transmission,*" McGraw-Hill Book Company, 1965.

9. R.E. Ziemer, W.H. Tranter, "*Principles of Communications - Systems, Modulation, and Noise,*" Second Edition, Houghton Mifflin Company, 1985.

10. P.L. Hunter, "*Converter Circuit and Method Having Fast Responding Current Balance and Limiting,*" U.S. Patent 4,002,963, 1977.

11. L.H. Dixon, "*Average Current-Mode Control of Switching Power Supplies,*" Unitrode Power Supply Design Seminar handbook, 1990, pp.5.1-5.14.

12. R.D. Middlebrook, S. Cuk, "*A General Unified Approach to Modeling Switching Converter Power Stages,*" IEEE Power Electronics Specialists Conference, 1984 Record, pp. 18-34.

13. S. Cuk, R.D. Middlebrook, "*A General Unified Approach to Modeling Switching DC-to-DC Converters in Discontinuous Conduction Mode,* " IEEE Power Electronics Specialists Conference, 1977 Record, pp. 36-57.

14. D. Maksimovic, S. Cuk, "*A Unified Analysis of PWM Converters in Discontinuous Modes,*" Power Conversion International Conference (PCI '89), 1989 Proceedings.

15. V. Vorpérian, "*Simplified Analysis of PWM Converters Using the Model of the PWM Switch: Parts I and II,*" IEEE Transactions on Aerospace and Electronic Systems, Vol. 26, No. 3, pp. 490-505, May 1990. See also VPEC Newsletter "Current," Fall 1988, and Spring 1989 Issues, Virginia Polytechnic Institute and State University.

16. F.C. Lee, M.F. Mahmoud, Y. Yu, "*Design Handbook for a Standardized Control Module for DC-to-DC Converters,*" Volume I, NASA CR-165172, April, 1980. See also F.C. Lee, Y. Yu, M.F. Mahmoud, "*A Unified Analysis and Design Procedure for a Standardized Control Module for DC-DC Switching Regulators,*" Power Electronics Specialists Conference, 1980 Record, pp.284-301.

17. S.Hsu, A.R. Brown, L Rensink, and R.D. Middlebrook, "*Modelling and Analysis of Switching DC-to-DC Converters in Constant-Frequency Current-Programmed Mode,*" IEEE Power Electronics Specialists Conference, 1979 Record, pp.284-301.

18. R.D. Middlebrook, "*Topics in Multiple-Loop Regulators and Current-Mode Programming,*" IEEE Power Electronics Specialists Conference, 1985 Record, pp. 716-732.

19. R.D. Middlebrook, "*Modeling Current-Programmed Buck and Boost Regulators,*" IEEE Transactions on Power Electronics, Vol. 4, No. 1, pp. 36-52, January 1990.

20. R. Martinelli, "*The Benefits of Multi-Loop Feedback,*" Power Conversion International Conference (PCI '87), 1987 Proceedings, pp.227-245.

21. G.K. Schoneman, D.M. Mitchell, "*Output Impedance Considerations for Switching Regulators with Current-Injected Control,*" IEEE Transactions on Power Electronics, pp. 25-35 Vol. 4., No. 1, January 1989

22. V.G. Bello, "*Using the SPICE2 CAD Package to Simulate and Design the Current-Mode Converter,*" Powercon 11, 1984 Record, Paper H-2.

23. L.H. Dixon, "*Closing the Feedback Loop,*" Appendix C, Unitrode Power Supply Design Seminar, pp. 2C1-2C18, 1983.

24. B. Holland, "*Modelling, Analysis and Compensation of the Current-Mode Converter,*" Powercon 11, 1984 Record, Paper H-2.

25. A.S. Kislovski, "*Controlled-Quantity Concept in Small-Signal Analysis of Switching Power Cells,*" IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-19, No. 3, pp. 438-446, May 1983.

26. A.S. Kislovski, "*Introduction to Dynamical Analysis of Switching DC-DC Converters,*" EWV Engineering, Loechliweg 47, 3048 Berne, Switzerland, January 1985.

27. G.C. Verghese, C.A. Bruzos, K.N. Mahabir, "*Averaged and Sampled-Data Models for Current Mode Control: A Reexamination,*" IEEE Power Electronics Specialists Conference, 1989 Record, pp. 484-491.

28. A.R. Brown, R.D. Middlebrook, "*Sampled-Data Modeling of Switching Regulators,*" Power Electronics Specialists Conference, 1981 Record, pp. 349-369.

29. A.R. Brown, "*Topics in the Analysis, Measurement, and Design of High-Performance Switching Regulators,*" PhD. Dissertation, California Institute of Technology, May 15, 1981.

30. F.C. Lee, R.P. Iwens, Y. Yu, "*Generalized Computer-Aided Discrete Time Domain Modeling and Analysis of DC-DC Converters,*" IEEE Power Electronics Specialists Conference, 1977 Record, pp. 58-69.

31. C.J. Hsiao, R.B. Ridley, F.C. Lee, "*Small-Signal Analysis of Switching DC-DC Converters Using the Simulation Program COSMIR,*" Virginia

Power Electronics Center Seminar, 1988 Record, pp. 219-226, Virginia Polytechnic Institute and State University.

32. B.Y. Lau, R.D. Middlebrook, "*Small-Signal Frequency-Response Theory for Two-Switched Network Piecewise-Constant DC-to-DC Converter Systems,*" Power Electronics Specialists' Conference, 1986 Record, pp. 186-199.

33. R.P.E. Tymerski, "*Frequency Analysis of Time-Interval-Modulated Switched Networks,*" Power Electronics Specialists' Conference, 1990 Record, pp. 355-362.

34. J.O. Groves, "*Small-Signal Analysis of Piecewise-Linear Circuits with Periodic Solutions,*" Virginia Power Electronics Center Seminar, 1990 Record, pp. 127-136, Virginia Polytechnic Institute and State University.

35. K.J. Astrom, B. Wittenmark, "*Computer Controlled Systems,*" pp. 66-79, Prentice-Hall, Inc., 1984.

36. R.D. Middlebrook, "*Predicting Modulator Phase Lag in PWM Converter Feedback Loops,*" Powercon 8, Paper H-4, April 27-30, 1981.

37. R. Redl, N.O. Sokal, "*Current-Mode Control, Five Different Types, Used with the Three Basic Classes of Power Converters: Small-Signal AC and Large-Signal DC Characterization, Stability Requirements, and Implementation of Practical Circuits,*" IEEE Power Electronics Specialists Conference, 1985 Record, pp. 771-785.

38. V. Vorpérian, "*Analysis of Resonant Converters*" PhD. Dissertation, California Institute of Technology, May 1984.

39. Unitrode Corporation, "*Linear Integrated Circuits Data Book,*" pp. 3.74-3.80, 1987.

40. B.H. Cho, F.C. Lee, "*Measurement of Loop Gain with the Digital Modulator,*" IEEE Power Electronics Specialists Conference, 1984 Record, pp. 363-373.

41. R.B. Ridley, "*Design of an Improved Digital Signal Modulator and Demodulator,*" Virginia Power Electronics Center Seminar, 1985 Record, pp. 4.47-4.65.

42. R.P.E. Tymerski, K.C. Daly, "*Modelling and Analysis of Current-Programmed DC/DC Converters,*" Journal of Electrical and Electronics Engineering, Australia, Vol 5, No. 1, March 1985, pp. 85-91.

43. P.W. Tuinenga, " *A Guide to Circuit Simulation and Analysis Using PSpice,*" Prentice-Hall, Inc., 1988.

A More Accurate Current-Mode Control Model

Dr. Ray Ridley
Ridley Engineering, Inc.

Abstract

For working power supply engineers, the Unitrode handbook is often the standard reference for control analysis. This paper gives a very simple extension to the existing Unitrode models that accounts for the subharmonic oscillation phenomenon seen in current-mode controlled converters. Without needing any complex analysis, the oscillation phenomenon, ramp addition, and control transfer function are unified in a single model.

I. Introduction

This paper provides the simple results needed to augment the existing single-pole model typically used for current-mode control. These results will allow you to:

1. Model and predict control transfer functions with greater accuracy.
2. Select the proper compensation ramp.
3. Use a single small-signal model for both transfer functions and current loop stabilization.
4. Decide when you need to add a ramp to your power circuit, and how much to add.

The analytical results presented here are the result of complex modeling techniques using sampled-data. Once armed with these equations understanding and designing your current loop becomes very simple. You don't need to be familiar with any of the more complex analysis techniques to get the full benefits of the extended model.

All of the analysis results presented here are incorporated in the Power 4-5-6 design software. This software makes it easy for you to use the latest and most accurate models for your power converter design and control.

Methods of implementing the compensating ramp in your circuit are also discussed. The usual methods suggested by the control IC manufacturers are not recommended for rugged and predictable operation.

II. Basic Current-Source Dynamics

The basic concept of current mode control is shown in Fig. 1.

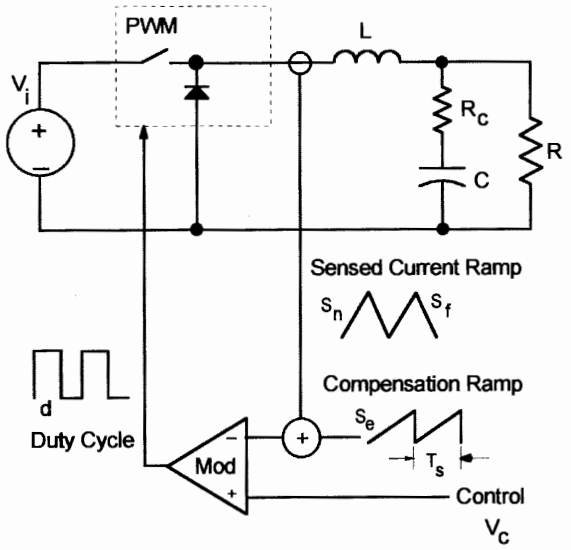


Fig. 1 – Peak current-mode control circuit.

Instead of using just a sawtooth ramp to control the duty cycle of the converter, a signal proportional to the inductor current is summed with a sawtooth ramp. In some

cases, the sawtooth ramp is omitted completely, and the error voltage signal, V_c, controls the peak value of the inductor current.

We don't usually sense the inductor current directly – it's often inconvenient or inefficient to do this. Usually, the power switch current is sensed to gather the information about the inductor current.

Early analyses of this control assumed ideal control of the current, and modeled the system by viewing the inductor as a controlled current source. This is the basis of the widely used models presented in an early paper [1] and Unitrode handbooks [2].

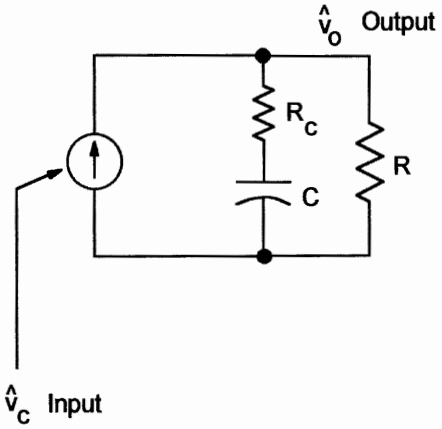


Fig. 2: Simplest small-signal model – current source feeding the load.

III. Subharmonic Oscillation

The current-source analogy works fine under many conditions, but with one problem: the system can oscillate! This is of course, well known and documented. And, we all know retaining the sawtooth compensating ramp in the control system eliminates the problem – but most small-signal models don't tell you what this does to the control characteristics.

Fig. 3: shows the nature of the current loop oscillation. At duty cycles approaching 50% and beyond, the peak current is regulated at a fixed value, but the current will oscillate back and forth on subsequent switching cycles.

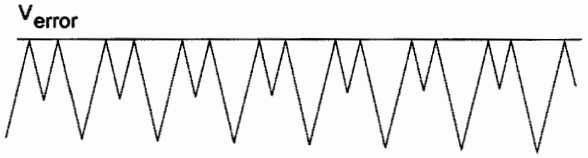


Fig. 3: Subharmonic oscillation waveforms.

The situation is really very simple, as pointed out by Holland [3] in an early paper – the current-mode oscillation is like any other oscillation – if it's undamped, it will continue to ring, and grow in amplitude under some conditions. If it's damped, the oscillations decrease and die out.

The sampled-data or discrete-time analysis of this phenomenon, required because of its high frequency, has been with us for some time. So why don't most engineers use this in their work? Because the analysis is usually too complex. However, it has been shown [4] that very practical results can be simplified into an easily usable form.

IV. Sampled-Data Analysis

Early modeling combined simple average analysis with separate explanations of how the current signal could become unstable. However, the small-signal model and physical explanation for instability were never reconciled until [4]. This paper expanded upon earlier work [5], but found a way to simplify the results into a more useful format.

Other analyses have subsequently analyzed the same issue. Many of these agree in the way the problem is tackled and provide supporting experimental data. Others disagree in the methods but still come to the same conclusions about the second-order oscillatory system that results. They are all consistent in the values derived.

That's good news – we don't need to get hung up in conflicting sampled-data modeling techniques, or debates about how to analyze a system, we can use the common design equations everyone agrees on, and get on with the job of getting product out of the door.

V. Dominant Pole Models

The equivalent control system diagram for current mode control is shown in Fig. 4. The inductor current feedback becomes an inner feedback loop. We are usually concerned with the transfer function from the control input shown to the output of the power converter. The input is typically the input to the duty cycle modulator, provided by the error amplifier output.

Most designers are familiar with the fact that the current feedback loop reduces the main dynamic of the system to a dominant single-pole type response. This is a result of viewing the inductor as a controlled current source rather than as a state of the system.

The results of existing analysis for the three main types of converter are summarized below.

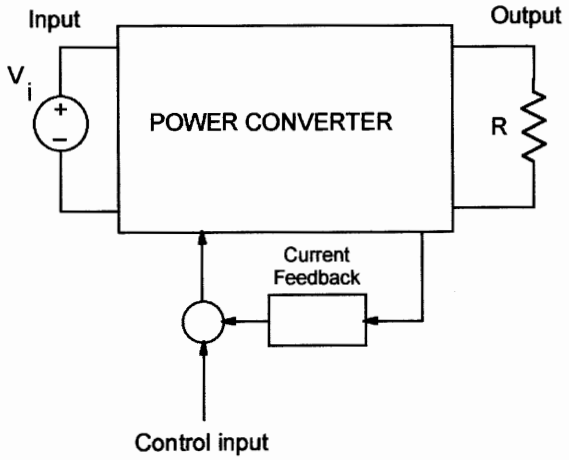


Fig. 4: Control system representation of current-mode control. Current loop is embedded in the system.

A. Buck Converter

The low-frequency model of the buck converter, commonly used by designers, and summarized in [2] is given by:

$$f_p(s) = K \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}}$$

The load resistor and capacitor determine the dominant pole, as we would expect for a current source feeding an RC network, shown in Fig. 3.

$$\omega_p = \frac{1}{RC}$$

In [4] there is a more accurate expression for the dominant pole of the buck, involving the external ramp and operating point of the converter:

$$\omega_p = \frac{1}{RC} + \frac{T_s}{LC}(m_c D' - 0.5)$$

However, this refinement is usually unnecessary. It only becomes important when too steep a ramp is used, showing how the pole can move. In most cases, the simplified form of the dominant pole is adequate for design purposes.

The power stage transfer function zero is determined by the equivalent series resistance of the capacitor:

$$\omega_z = \frac{1}{R_c C}$$

This expression for the output capacitor zero is the same for all the converters.

B. Boost Converter

The boost converter has an additional term in the control transfer function, caused by the right-half-plane (rhp) zero of the converter:

$$f_p(s) = K \frac{\left[1+\frac{s}{\omega_z}\right]\left[1-\frac{s}{\omega_{z\,rhp}}\right]}{1+\frac{s}{\omega_p}}$$

The dominant pole is located at

$$\omega_p = \frac{2}{RC}$$

and the rhp zero is at

$$\omega_{z\,rhp} = \frac{R(1-D)^2}{L}$$

Note that the rhp zero expression is exactly the same as that for voltage mode control. Using current mode does not move this at all, although it is easier to compensate for since we do not also have to deal with the double pole response of the LC filter that is present with voltage mode control.

C. Flyback Converter

The flyback converter also has a rhp zero term in the control transfer function:

$$f_p(s) = K \frac{\left[1+\frac{s}{\omega_z}\right]\left[1-\frac{s}{\omega_{z\,rhp}}\right]}{1+\frac{s}{\omega_p}}$$

with the dominant pole determined by

$$\omega_p = \frac{1+D}{RC}$$

and the rhp zero at:

$$\omega_{z\,rhp} = \frac{R(1-D)^2}{DL}$$

As with the boost converter, this zero location is the same as for voltage mode control.

VI. Measured High-Frequency Effects

To account for the observed oscillation in the current mode system, we need to add a high-frequency correction term to the basic power stage transfer functions.

The converter transfer functions are modified from the above section by

$$f_p'(s) = f_p(s) f_h(s)$$

Without even considering the sampled-data type analysis, we can see what the form of the transfer function has to be. One way it becomes clear is to measure the control-to-output transfer functions, while adding different amounts of compensating ramp to the system.

Fig. 5 shows measurements of power stage transfer functions plotted beyond half the switching frequency. The characteristic at half the switching frequency is a classic double pole response that can be seen in any fundamental text on bode plots and control theory.

These curves are for a buck converter operating at a 45% duty cycle. In the upper curve, there is no compensating ramp added, and there is a sharp peak in the transfer function at half the switching frequency.

The curves below this have increasing amounts of compensating ramp added to them, until the bottom curve is reached and the double poles are overdamped.

Once you make this series of measurements, the need for the correction to the power stage transfer function becomes obvious.

Mathematical theoreticians may argue that measuring and predicting transfer functions up to this frequency is of questionable analytical merit. However, there is such a direct correlation between the measurements and the oscillatory behavior of the system, that the correction term is vital for good and practical modeling.

When the system transfer function peaks with a high Q, the inductor current oscillates back and forth, as shown in Fig. 6. When the transfer function is well damped, the inductor current behaves, returning quickly to equilibrium after an initial disturbance.

Including this high frequency extension in the model is a very practical and powerful tool – it has real meaning to the designer.

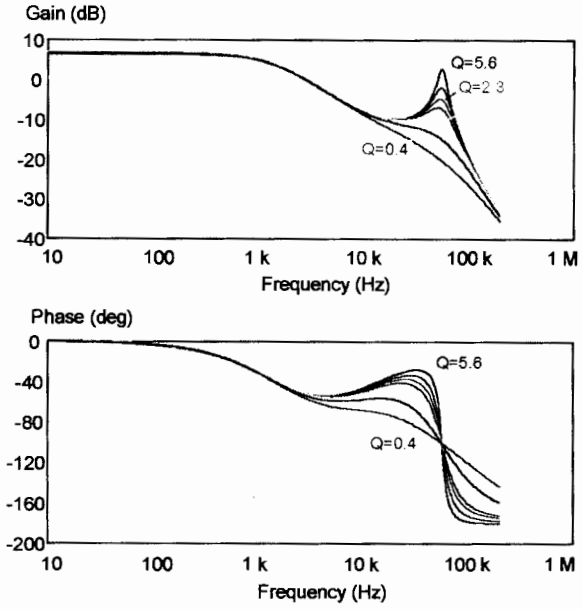


Fig. 5: Power stage transfer functions plotted up to the switching frequency. Notice the obvious double-pole characteristic centered at half the switching frequency.

Fig. 6: Inductor current oscillation waveforms. Waveforms correspond to a Q of 7.6, 5.6, 2.3 and 0.7.

VII. Analytical Results

The qualitative understanding of the double poles is obvious. Quantitative analysis via sampled-data, or other methods gives the simple transfer function parameters to be used for design.

The high frequency term is a common expression for all given by

$$f_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}}$$

where the double-pole oscillation is at half the switching frequency.

$$\omega_n = \frac{\pi}{T_s}$$

The damping is given by

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)}$$

The compensation ramp factor is given by

$$m_c = 1 + \frac{s_e}{s_n}$$

where the compensating ramp slope, se, is

$$s_e = \frac{V_{p-p}}{T_s}$$

and the slope of the sensed current waveform into the PWM controller is

$$s_n = \frac{V_{on}}{L} R_i$$

R_i is the gain from the inductor current to the sensed voltage fed into the control PWM, and V_{on} is the voltage across the inductor when the switch is on. For a simple nonisolated converter with resistive sensing, R_i is the value of the sense resistor.

These equations are useful for anyone wanting to model their converter and predict its response. They will give much more accurate results than simple single-pole models.

For those not interested in modeling, who don't have time and just need to get on with building a converter, the equations give you

the information you need for design, as explained in the next section.

VIII. How Much Ramp?

So what do you need to do with this information? The answer is simple – make sure your current loop won't oscillate. Or, in small-signal analysis terms, make sure the Q of the double pole is one or less. And how do you do this? Just by adding a compensating ramp, as all previous papers advise.

How much ramp do you add? Well, going by the small-signal theory, we just set the Q of the double poles to one, and solve the resulting system. Most early publications express the amount of ramp added in terms of the off-time ramp slope, S_f. If we solve the equation for Q_p in the same terms, the result is:

$$\frac{s_e}{s_f} = 1 - \frac{0.18}{D}$$

This is not quite the same as other suggestions. Some publications recommend adding as much ramp as the downslope. This is more than is needed, overdamping the system.

Others suggest adding half as much ramp as the downslope of the inductor current. For the buck converter, in theory, this cancels all perturbations from input to output. In practice, this nulling is never achieved completely, a small amount of noise makes it impossible.

Another question is when should you start adding a ramp to a system? Earlier simplistic analysis says that no ramp is needed until you reach a 50% duty cycle. There is something troubling about this. A power supply is an analog circuit. It would be a little strange if it were fine at 49.9% duty cycle, and unstable at 50.1%. The analog world just does not behave that way. In the real world, you often need to start adding a compensation ramp well before a 50% duty cycle is reached.

The design equation above continues to add ramp down to an 18% duty cycle in order to keep the Q_p of the current-mode double pole equal to 1. This is probably overly conservative – a more practical value for starting to add a compensating ramp is at D=36%.

IX. Instability at Less Than 50% Duty

Many publications, especially those from the manufacturers of control chips, explicitly tell you that you don't need to use a compensating ramp in the circuit at duty cycles less than 50%. This conflicts with the suggestions given above.

So what should you do? There are some special circuit conditions that cause this seeming contradiction in analysis results.

First, remember that the current loop oscillation is *only* a problem with continuous conduction operation (CCM) near or above 50% duty cycle. Many converters are operated in discontinuous conduction mode (DCM), especially flyback converters that are the most popular choice for low power outputs.

Secondly, if you choose to use a control chip such as the UC1842, this chip has a *maximum* duty cycle capability of just under 50%. That does not mean that the converter will ever operate in that region – typically it will never see more than perhaps a 40% duty cycle. More often than not, this will not be a severe problem.

But sometimes, with low input line, you will operate a converter close to 50%, and you may need to add ramp to compensate the current loop. Consider a case of a 44% duty cycle. The double pole peaking is determined by

$$Q_p = \frac{1}{\pi(0.56 - 0.5)} = 5.6$$

This can get you into trouble. Look at the power stage gain (lower curve) in Fig. 7. The peaking on this curve corresponds to a Q_p of

5.6. With just the current feedback loop closed, the system is stable – the current will bounce back and forth, but the oscillations eventually die down, as shown in Fig. 8.

Now consider what happens when the voltage regulation loop is closed. With a crossover frequency of 14 kHz (reasonable for a 110 kHz converter), the phase margin at this initial crossover frequency is close to 90 degrees.

But the loop gain crosses over the 0 dB axis *again* just before half the switching frequency, this time with no phase margin at all. The waveforms of Fig. 9 are the result – severe oscillation in the current loop.

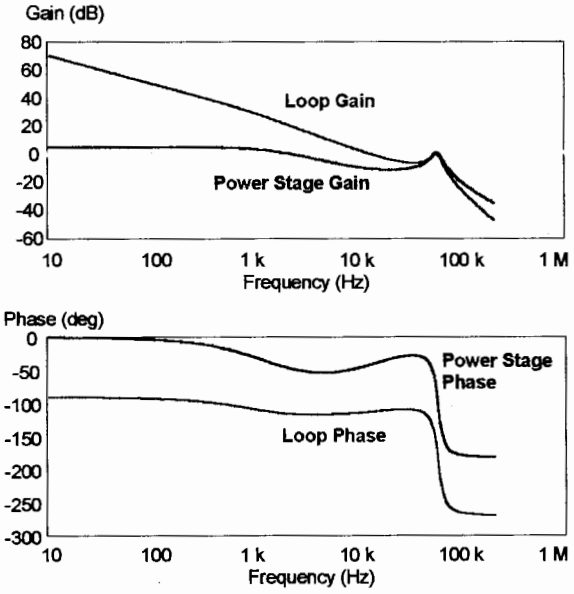


Figure 7: Current mode instability at less than 50% duty cycle. Adding compensation to the power stage transfer function causes the resulting loop gain to peak up and crossover again at half the switching frequency.

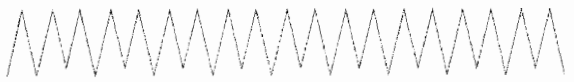


Figure 8: Inductor current waveforms at D=0.44 with only the current loop closed.

Figure 9: Inductor current waveforms at D=0.44, with outer feedback loop closed. System is now unstable, as shown by the loop gain of Fig. 7. A plot without the double pole extension to the model does not predict this oscillation.

This example clearly shows why the high-frequency extension is needed to the model. Without it, the current loop oscillation at less than 50% duty cycle cannot be predicted.

X. Magnetizing Ramp Addition

Some readers of this may say – "I've built converters at 45% duty cycle before and never had any problem – what's the issue here?" And they are quite correct. If you are building any kind of forward converter, or other isolated buck-derived topology, and sensing on the primary switch side, you often get a free ramp.

The magnetizing current of the main power transformer contributes a signal in addition to the reflected output inductor current, and this works in exactly the same way as the compensating ramp. The amount of slope contributed by the magnetizing current is given by

$$s'_e = \frac{V_i}{L_M} R_i$$

You should always check this value when doing your design. In most cases, the amount of ramp that you get due to the magnetizing current is more than enough to damp the double pole properly. In fact, the opposite is frequently true – the amount of ramp can often be excessive, especially for converters with low output ripple current, and the system can be very overdamped. This creates additional phase delay in the control to output

transfer function, as can be seen in Fig. 5 in the lowermost curve.

XI. How to Add the Ramp

A comment on ramp addition from field experience rather than the chip manufacturer's viewpoint is appropriate. This is a topic frequently dismissed as trivial, but it is very important if you want to get the best performance out of your current-mode system.

Ridley Engineering has taught control design courses, both theoretical, and hands- on for many years [6]. In designing current-mode control test circuits for these labs, we observed that the predicted and measured responses do not match well at all with conventional schemes for adding a ramp to a converter.

The simplest proposed method for ramp addition is to resistively sum the clock sawtooth signal with the sensed current signal shown in Fig. 10. This must be done with a high value of resistor in order not to overload the somewhat delicate clock signal. It provides a high-impedance, noise-susceptible signal for use by the control comparator.

It also connects additional components to the clock pin, and will affect the clock waveforms.

The sensitivity of the clock pin cannot be stressed enough. The Unitrode application notes tell you to put the timing capacitor close to the chip, but they do not emphasize this as much as perhaps they should. The timing capacitor is the most crucial component in the control circuit, and it should be placed first during layout, as physically close to the pins of the control chip as can be achieved.

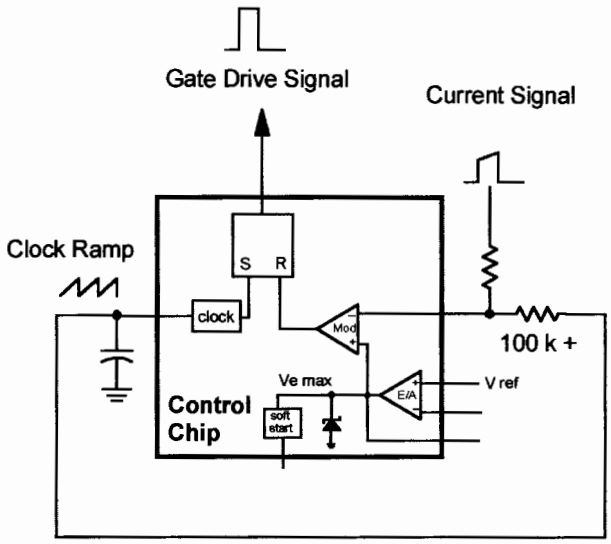


Figure 10: Resistive summing of the timing ramp and current signal for ramp addition. This circuit is NOT recommended. The clock signal is very sensitive to loading and noise, and can lead to power supply failure if it is corrupted.

If you don't do this, the results can be catastrophic. On one low-power off line converter, the timing capacitor was placed ¼" away from the pins, without a ground plane. When the converter was started up, the clock signal picked up switching noise, and briefly ran at 1 MHz instead of the desired 100 kHz. The resulting stress on the power switch was sufficient to cause failure. Moving the capacitor closer to the IC pins cured the problem.

Given this level of sensitivity, it is a good idea not to use the clock signal for *anything* except its intended purpose. Any additional components connected to the timing capacitor introduce the potential for noise into that node of the circuit. Even the buffered clock signal technique, shown in Fig. 11, can cause problems.

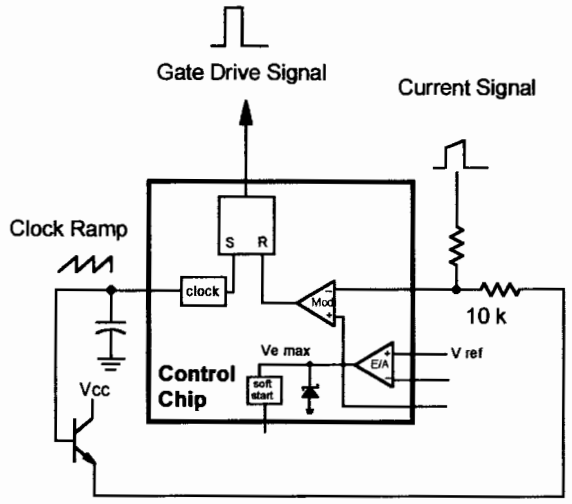


Figure 11: Buffered signal adding the timing ramp and current signal for ramp addition.This allows a lower summing resistor and better noise immunity. However, it is still not recommended to load the clock, even with a transistor.

An alternative approach to generating the ramp signal for current-mode compensation is shown in Fig. 12. This method uses the output drive signal, loaded with an RC network, to generate a compensation ramp to sum with the current mode signal.

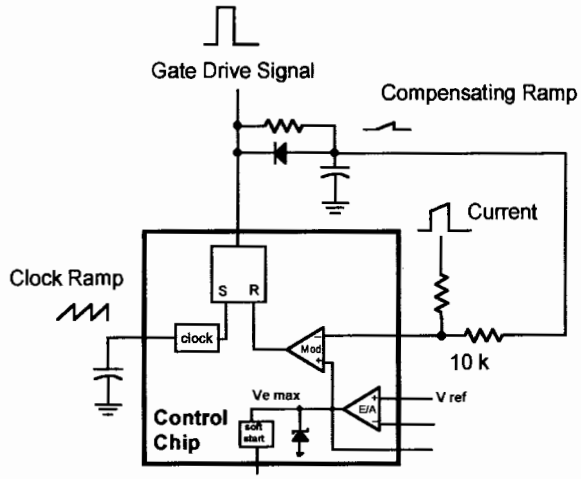


Figure 12: The best way to generate the compensation ramp is independently from the clock signal. The output gate drive signal provides a convenient way to do this.

XII. Conclusions

A simple extension to the common single-pole models can greatly enhance the accuracy and usefulness of current-mode control modeling. This allows you to design your power supply for peak performance.

Simple equations help you to select the proper ramp for compensating the current feedback loop, and to predict the correct control-to-output voltage transfer function. These equations show how a current-mode power supply can sometimes go unstable - even at duty cycles less than 50%.

Correlation between measured transfer functions, up to half the switching frequency, and observed circuit oscillations or jitter are very good.

Actual circuit implementation of the compensating ramp should be done very carefully. The clock signal should *not* be used for this function if you want to design the most rugged and reliable power supply.

Generating a low-noise compensating ramp will also provide a power supply with measurements that closely agree with predictions. This is a crucial factor in many industries, such as aerospace, where the customer expects delivered product and accurate circuit models.

Ray Ridley has specialized in the modeling, design, analysis, and measurement of switching power supplies for over 20 years. He has designed many power converters that have been placed in successful commercial production. In addition he has consulted both on the design of power converters and on the engineering processes required for successful power converter designs.

Ridley Engineering, Inc. is a recognized industry leader in switching power supply design, and is the only company today offering a combination of the most advanced application theory, design software, design hardware, training courses, and in-depth modeling of power systems.

References

1. C.W. Deisch, *"Switching Control Method Changes Power Converter into a Current Source"*, IEEE Power Electronics Specialists Conference, 1978 Record, pp. 300-306

2. Unitrode Power Supply Design Seminar SEM700, 1990, Appendix B.

3. B. Holland, *"Modeling, Analysis and Compensation of the Current-Mode Converter"*, Powercon 11, 1984 Record, Paper H-2.

4. R.B. Ridley, *"A New Small-Signal Model for Current-Mode Control"*, PhD Dissertation, Virginia Polytechnic Institute and State University, November, 1990. (Full version can be ordered, and the condensed version downloaded from the web site below.)

5. A.R. Brown, *"Topics in the Analysis, Measurement, and Design of High-Performance Switching Regulators"*, PhD. Dissertation, California Institute of Technology, May 15, 1981.

6. Ridley Engineering, Inc. *"Modeling and Control for Switching Power Supplies"* professional engineering seminar taught semi-annually. See [8].

7. Switching power supply design information, design tips, frequency response analyzers, and educational material for power supplies can be found at the web site located at: **http://www.ridleyengineering.com**